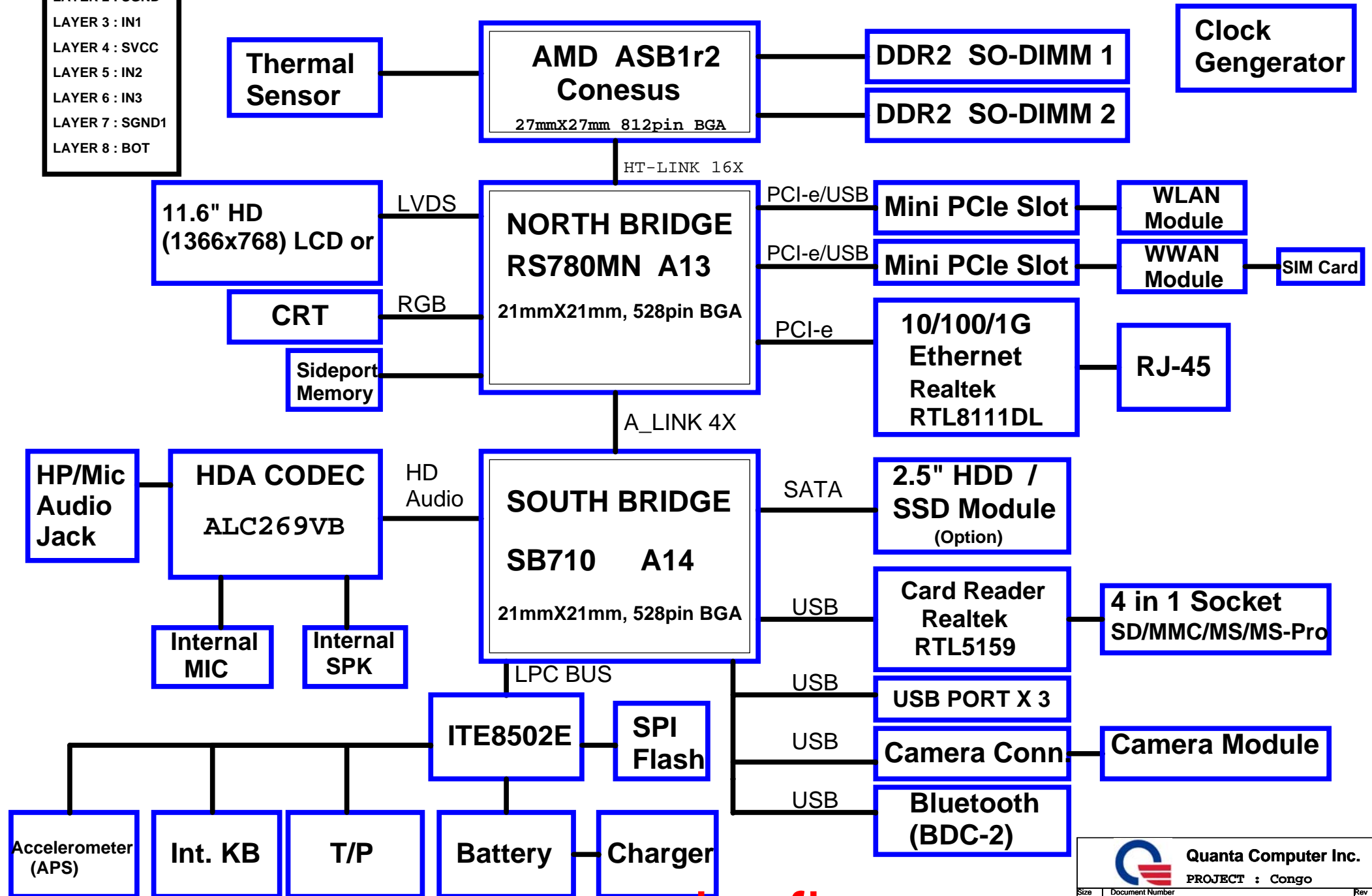
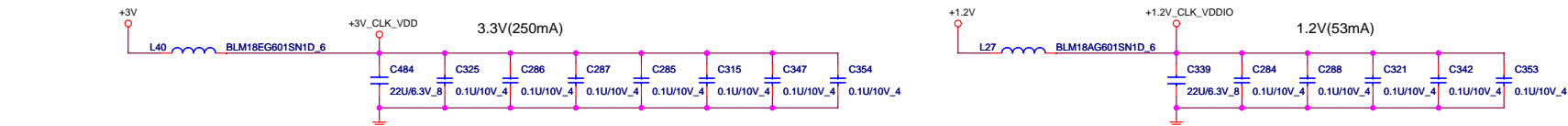


MK-Note Block Diagram -- AMD CONGO

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : SVCC
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : SGND1
LAYER 8 : BOT

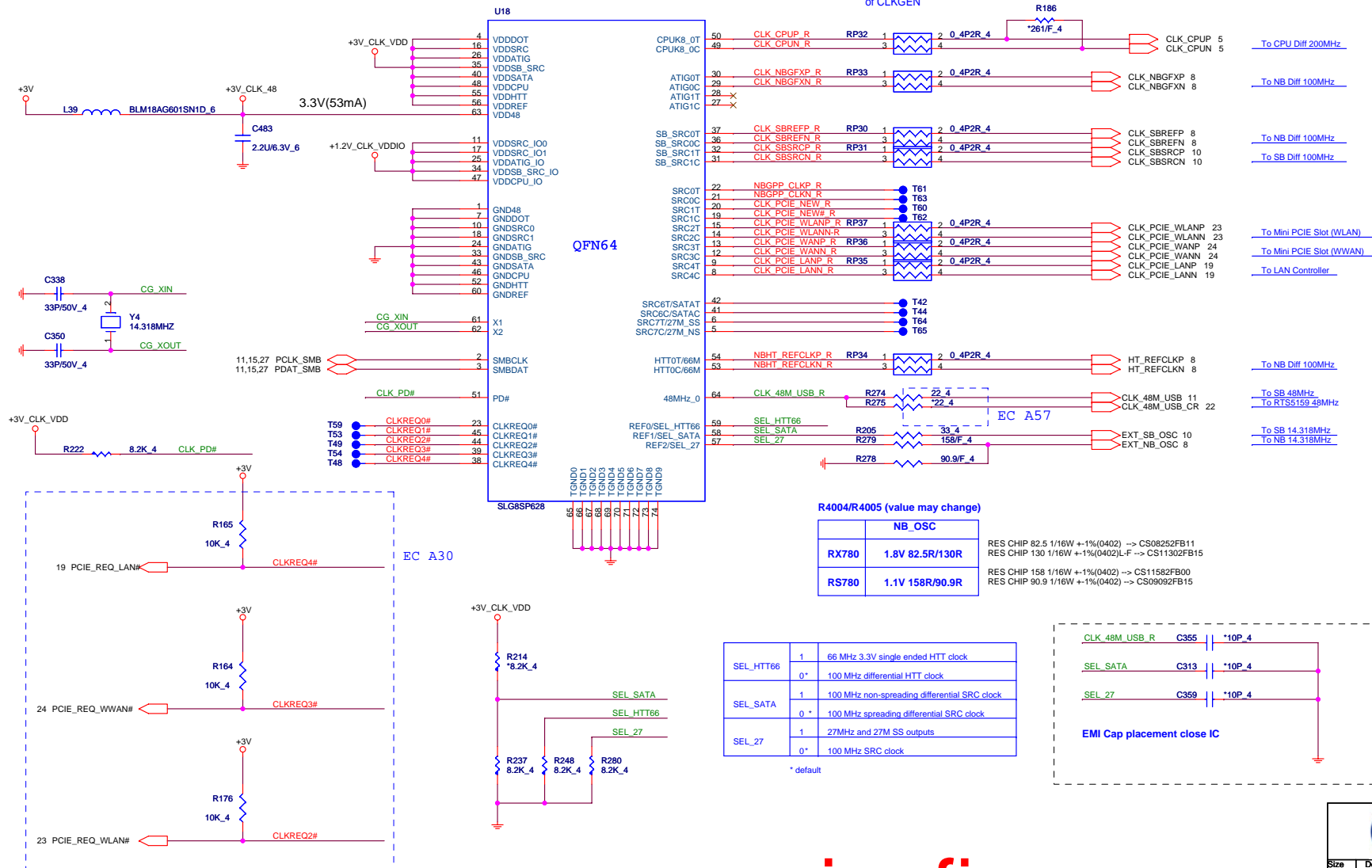




ICS9LPRS480 P/N : ALPRS480000
 SLG8SP628 P/N : AL8SP628000
 RTM880N-796 P/N : AL000880000

Clock chip has internal serial terminations
 for differential pairs, external resistors are
 reserved for debug purpose.

Place within 0.5"
 of CLKGEN



NB CLOCK INPUT TABLE

NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF (IN/OUT)
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF

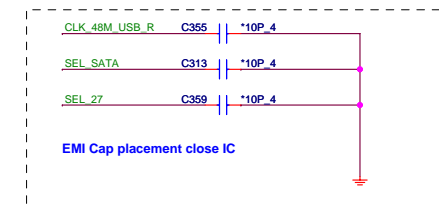
R4004/R4005 (value may change)

	NB_OSC
RX780	1.8V 82.5R/130R
RS780	1.1V 158R/90.9R

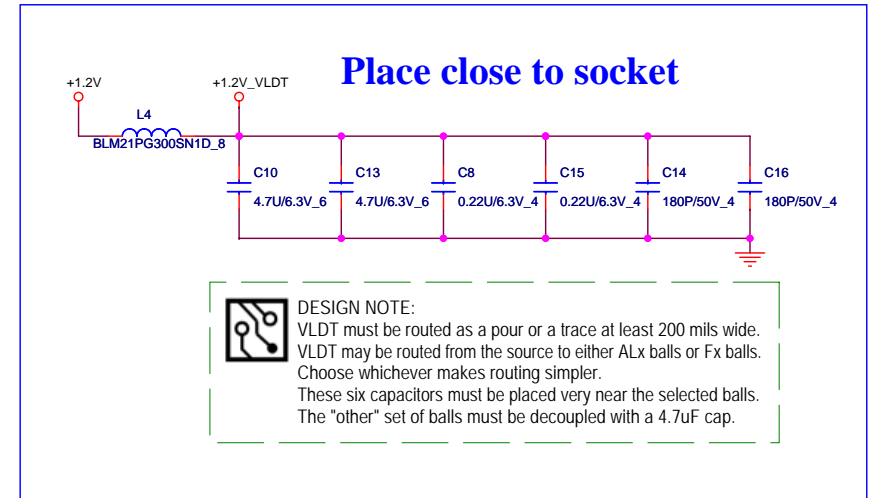
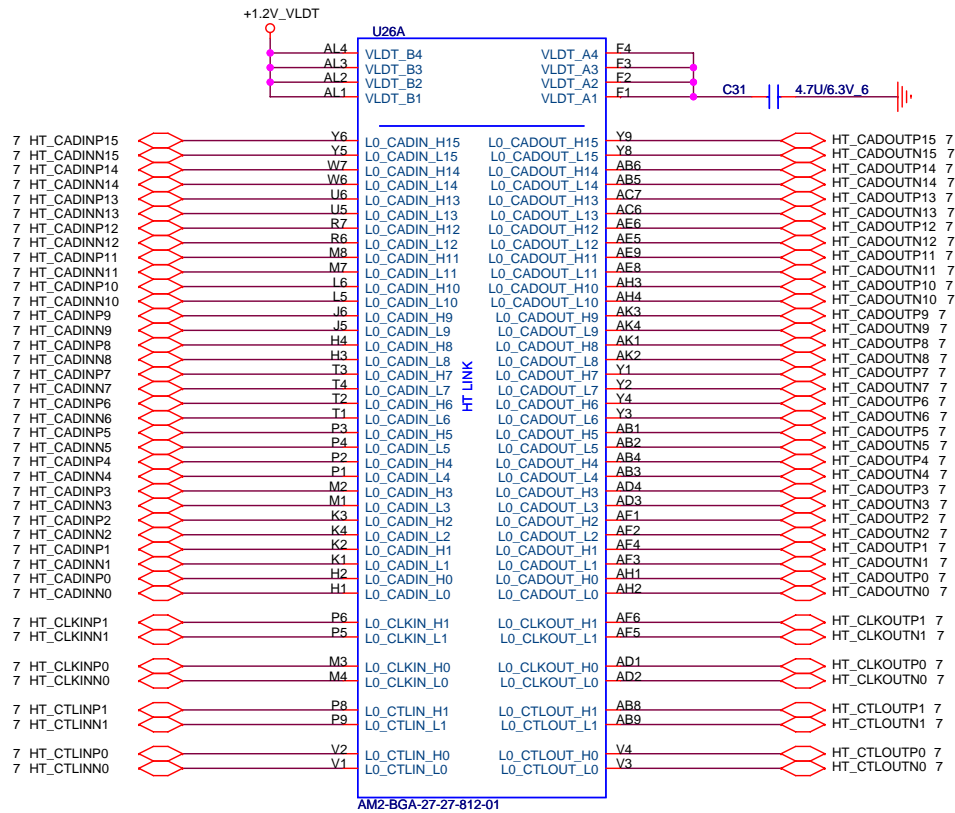
RES CHIP 82.5 1/16W +/-1%(0402) -> CS08252FB11
 RES CHIP 130 1/16W +/-1%(0402)LF -> CS11302FB15
 RES CHIP 158 1/16W +/-1%(0402) -> CS11582FB00
 RES CHIP 90.9 1/16W +/-1%(0402) -> CS09092FB15

SEL_HTT66	1 66 MHz 3.3V single ended HTT clock
SEL_HTT66	0* 100 MHz differential HTT clock
SEL_SATA	1 100 MHz non-spreading differential SRC clock
SEL_SATA	0* 100 MHz spreading differential SRC clock
SEL_27	1 27MHz and 27M SS outputs
SEL_27	0* 100 MHz SRC clock

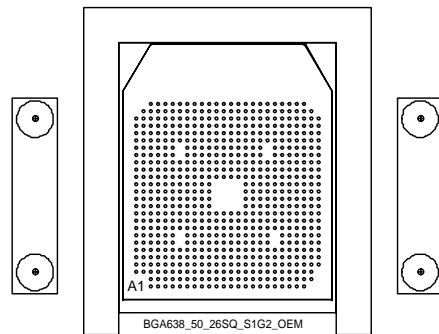
* default



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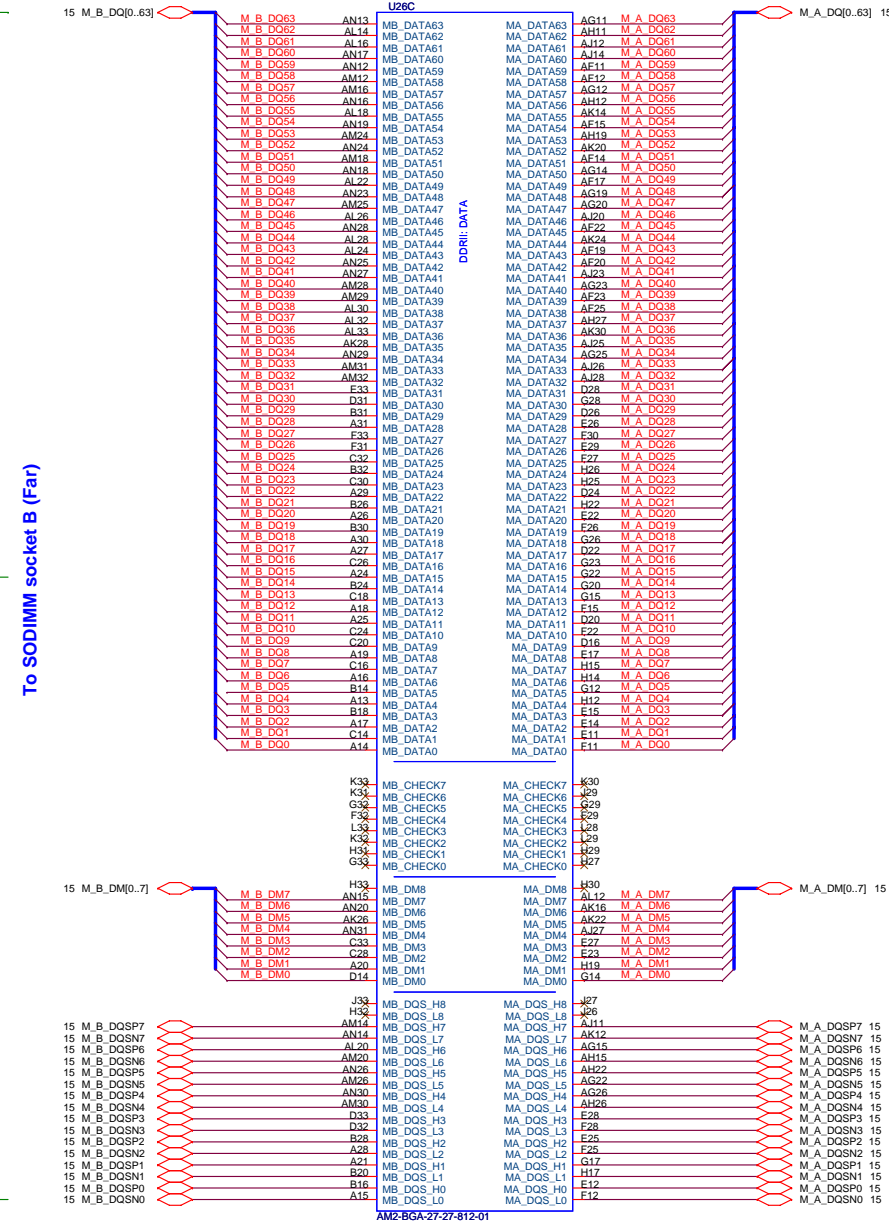
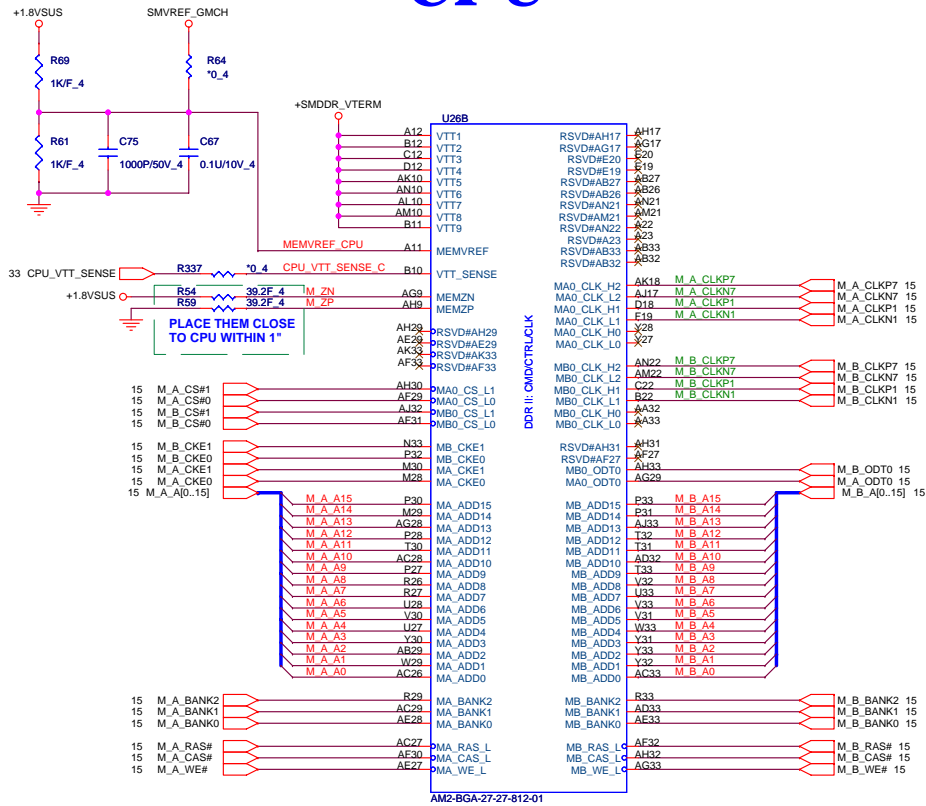


CPU

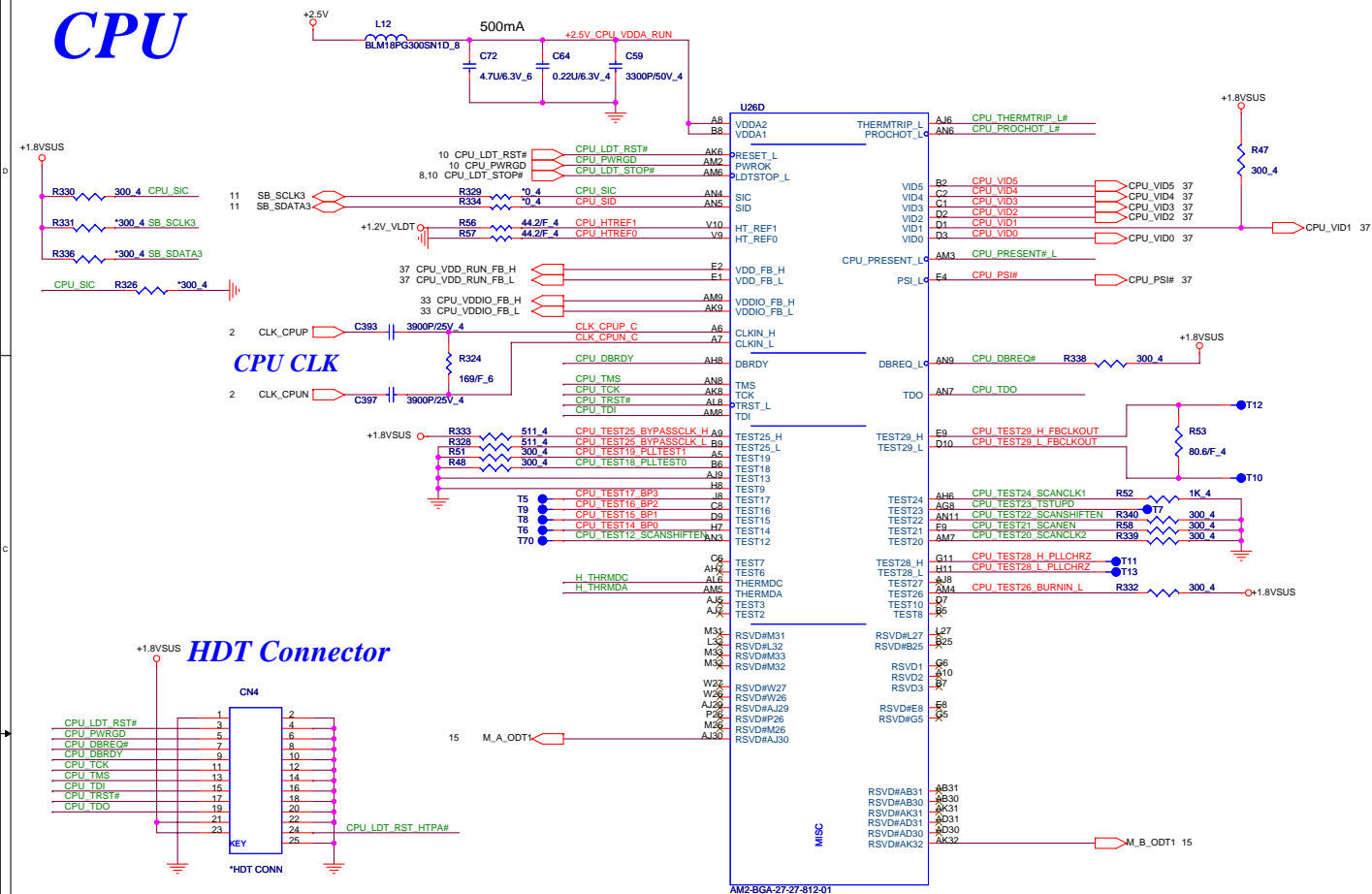


CPU

Processor Memory Interface

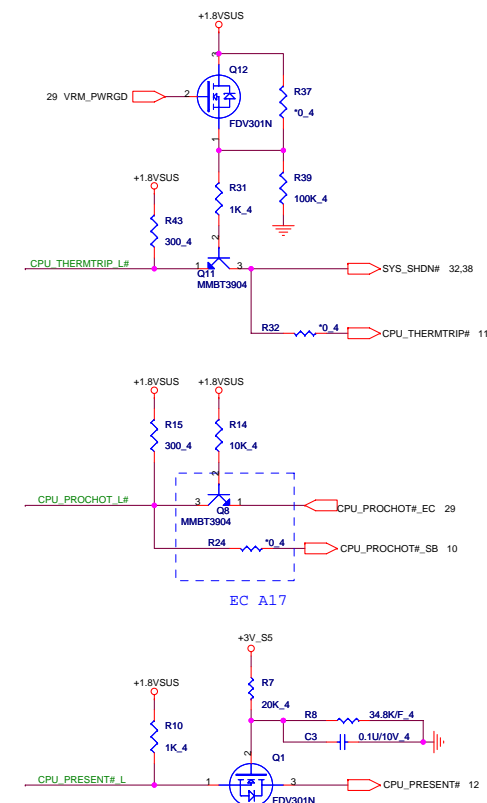


CPU

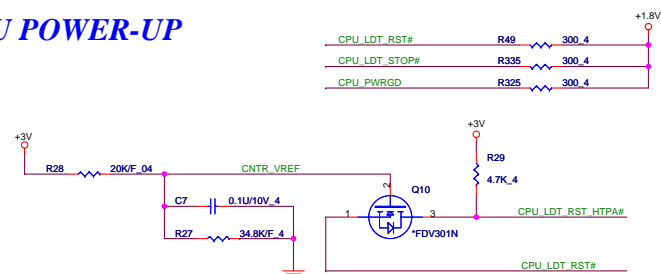


CPU THERM

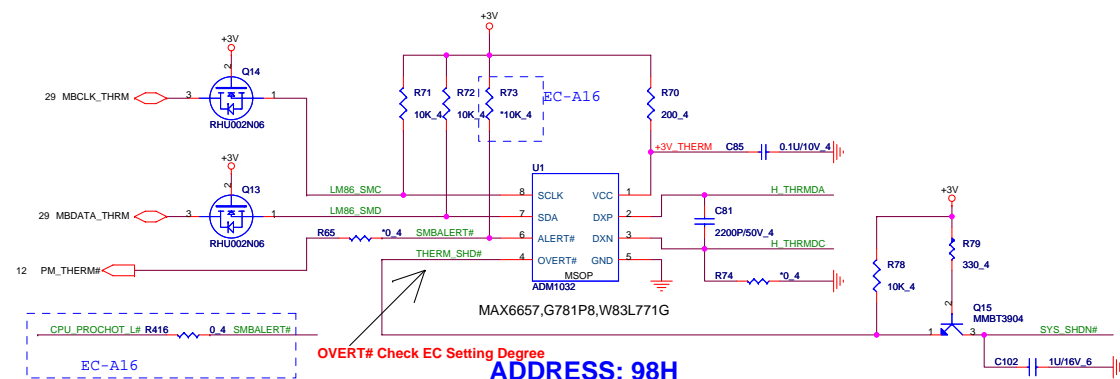
05

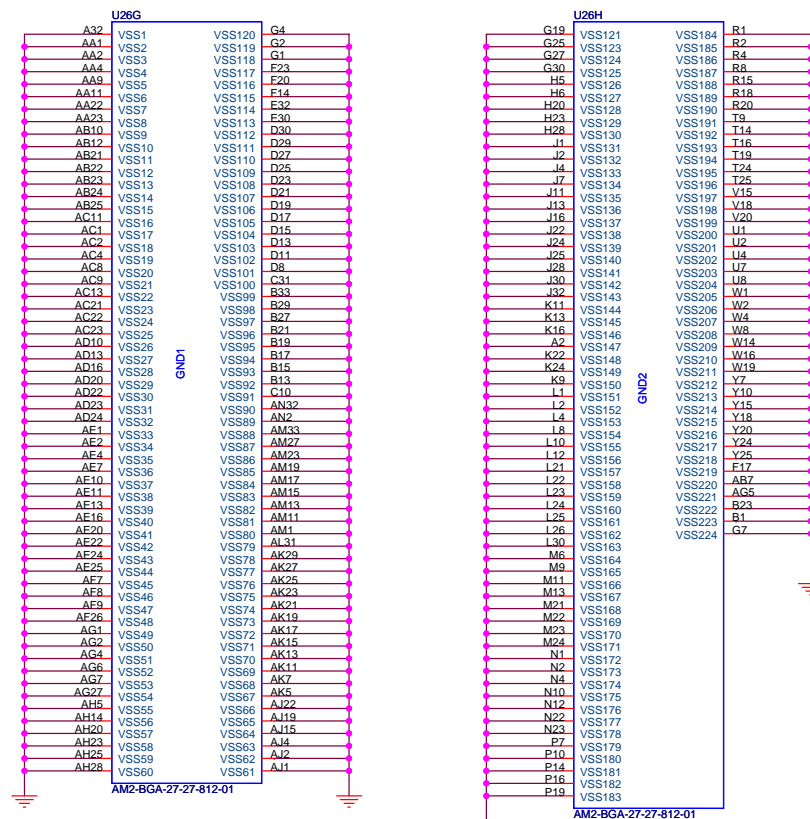
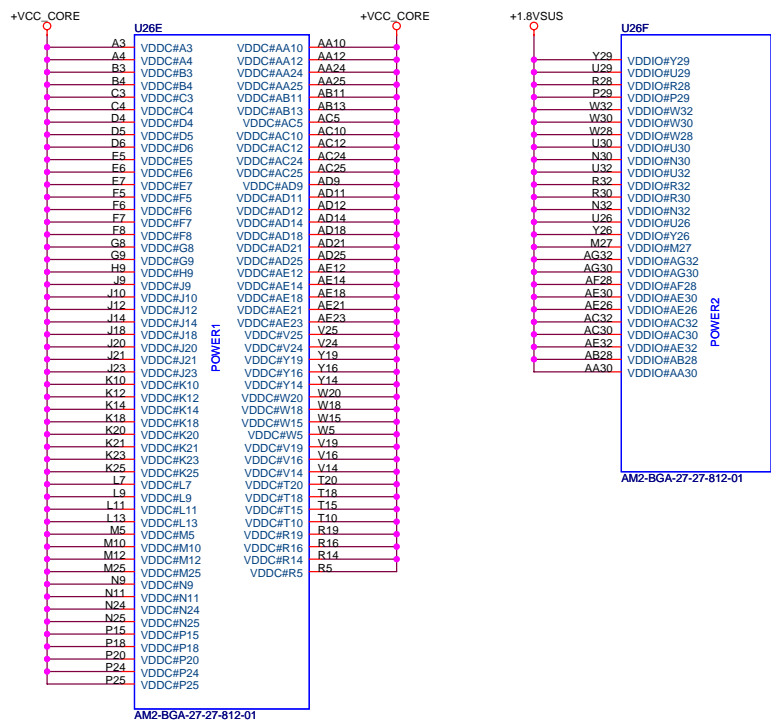


CPU POWER-UP



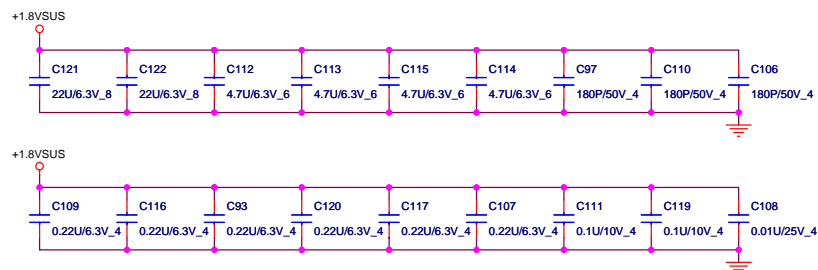
CPU H/W MONITOR



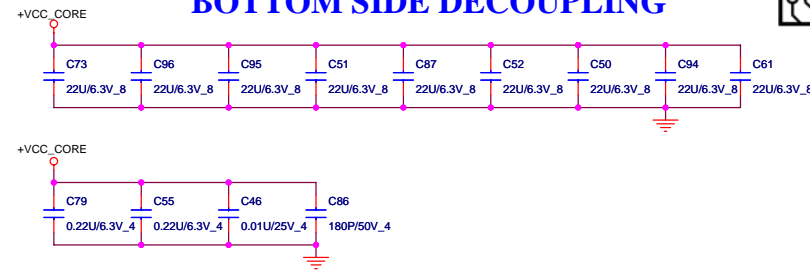


PROCESSOR POWER AND GROUND

DECOUPLING BETWEEN PROCESSOR AND DIMMs PLACE CLOSE TO PROCESSOR AS POSSIBLE



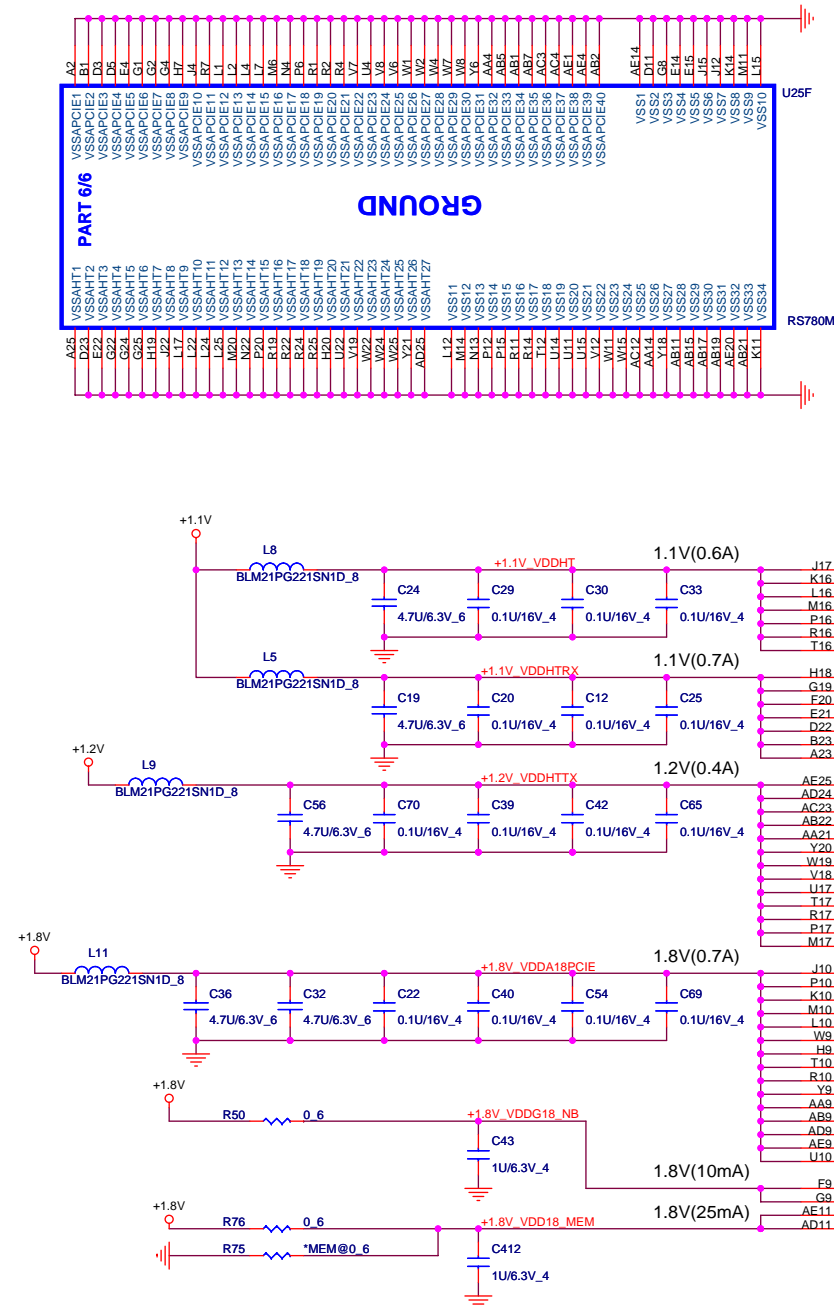
BOTTOM SIDE DECOUPLING





RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDDG18	+1.8V	+1.8V	+1.8V	PLLVD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V/1.5V	NC	+1.8V/1.5V	VDDLTP18	+1.8V	NC	+1.8V
VDDG33	+3.3V	NC	+3.3V	VDDL18	+1.8V	NC	+1.8V
IOPLLVD18	+1.8V	NC	+1.8V	VDDL18	+3.3V	NC	NC



PART 5/6

POWER

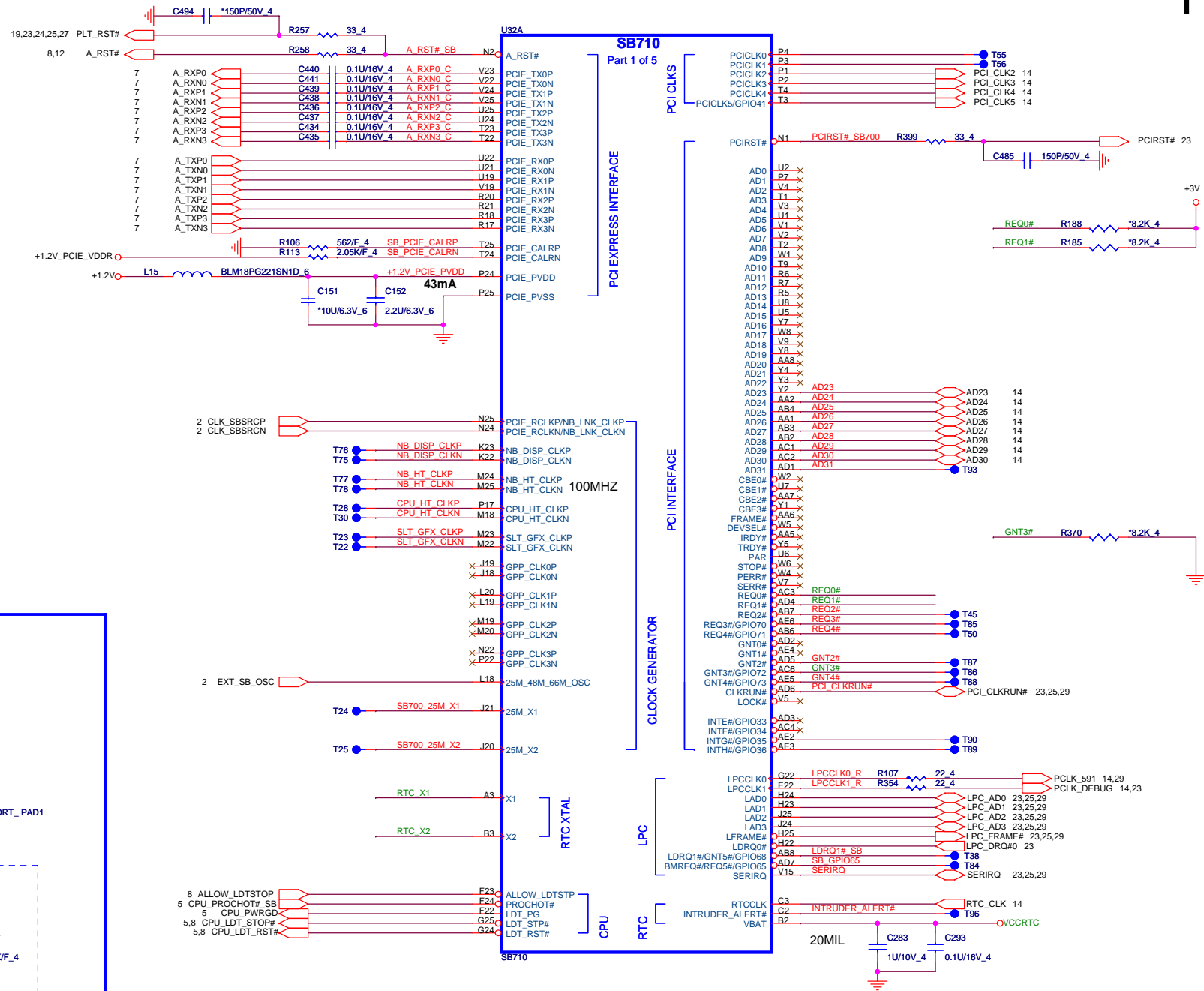
RS780

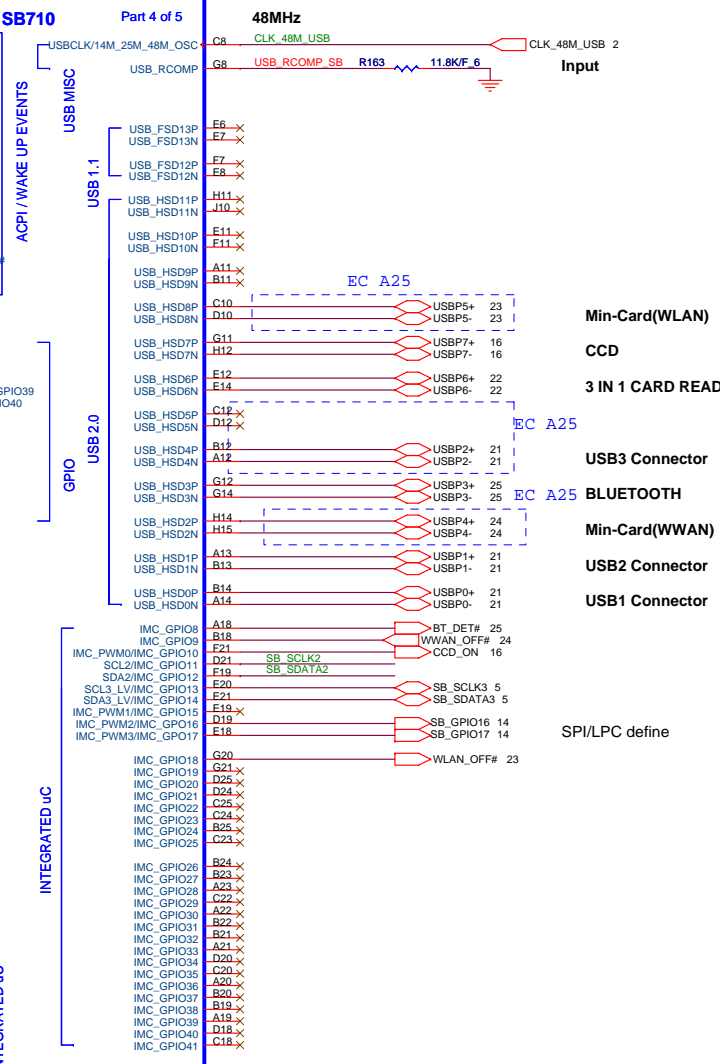
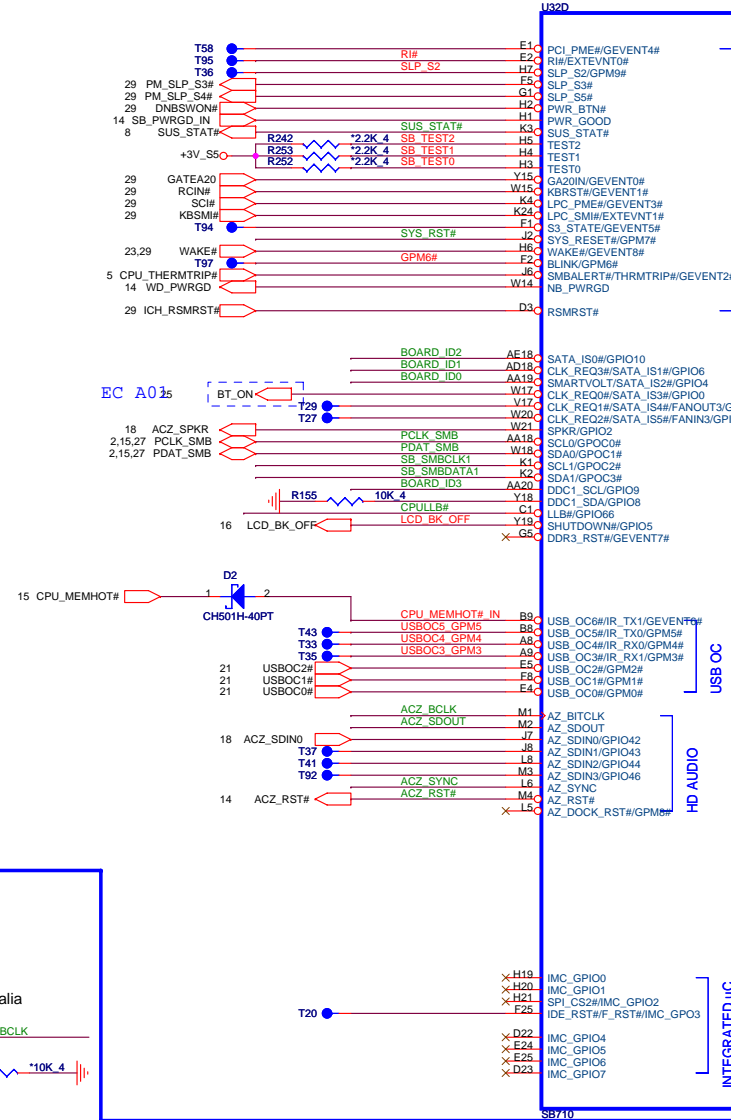
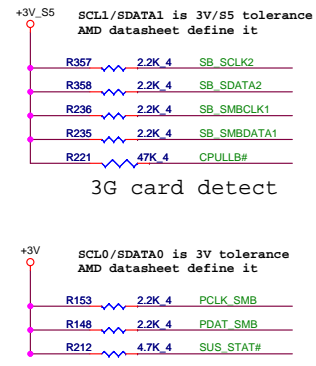
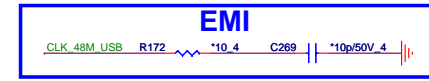
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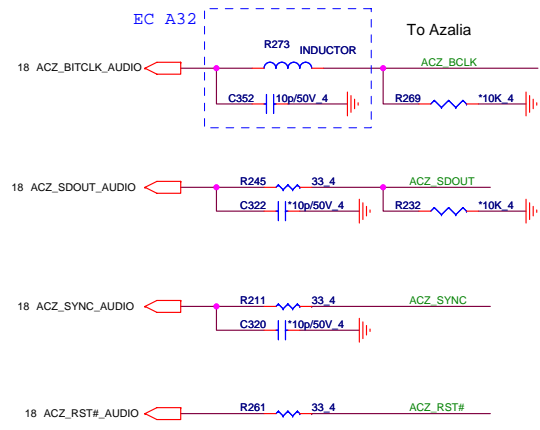
Size	Document Number	Rev
	RS780-POWER/GND 3/3	1A
Date:	Thursday, October 22, 2009	Sheet 9 of 42





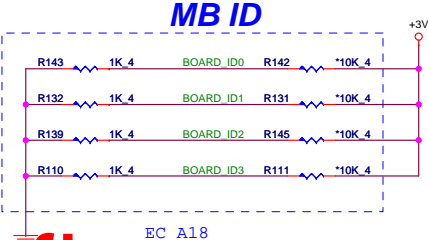
- 48MHz
- CLK 48M_USB
- USB_RCOMP
- USB_FSD13P
- USB_FSD13N
- USB_FSD12P
- USB_FSD12N
- USB_HSD11P
- USB_HSD11N
- USB_HSD10P
- USB_HSD10N
- USB_HSD9P
- USB_HSD9N
- USB_HSD8P
- USB_HSD8N
- USB_HSD7P
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- USB_HSD0P
- USB_HSD0N
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- IMC_GPIO9
- IMC_GPIO10
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- IMC_GPIO36
- IMC_GPIO37
- IMC_GPIO38
- IMC_GPIO39
- IMC_GPIO40
- IMC_GPIO41
- BT_DET#
- WWAN_OFF#
- CCD_ON
- SB_SCLK2
- SB_SDATA2
- SB_SCLK3
- SB_SDATA3
- SB_GPIO16
- SB_GPIO17
- WLAN_OFF#

HD Audio Interface



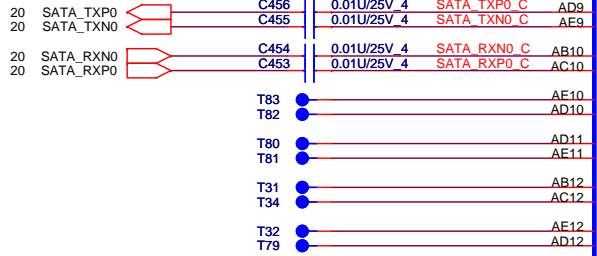
MB ID Selection Table

BOARD_ID	BOARD_ID0	BOARD_ID1	BOARD_ID2	BOARD_ID3
DV	H	H	H	H
SIT	L	L	L	L
SVT	L	L	L	H
SOVP	L	L	H	L



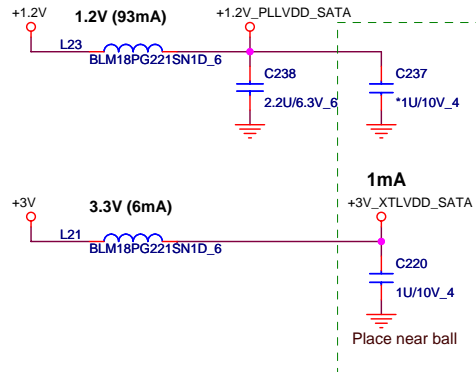
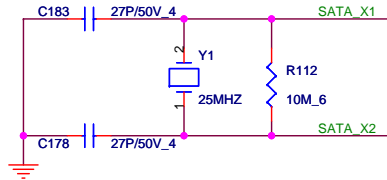
PLACE SATA AC COUPLING CAPS CLOSE TO SB700

SATA HDD



NOTE:

Resistor IS 1K 1% FOR 25MHZ XTAL, 4.99K 1% FOR 100MHZ INTERNAL CLOCK



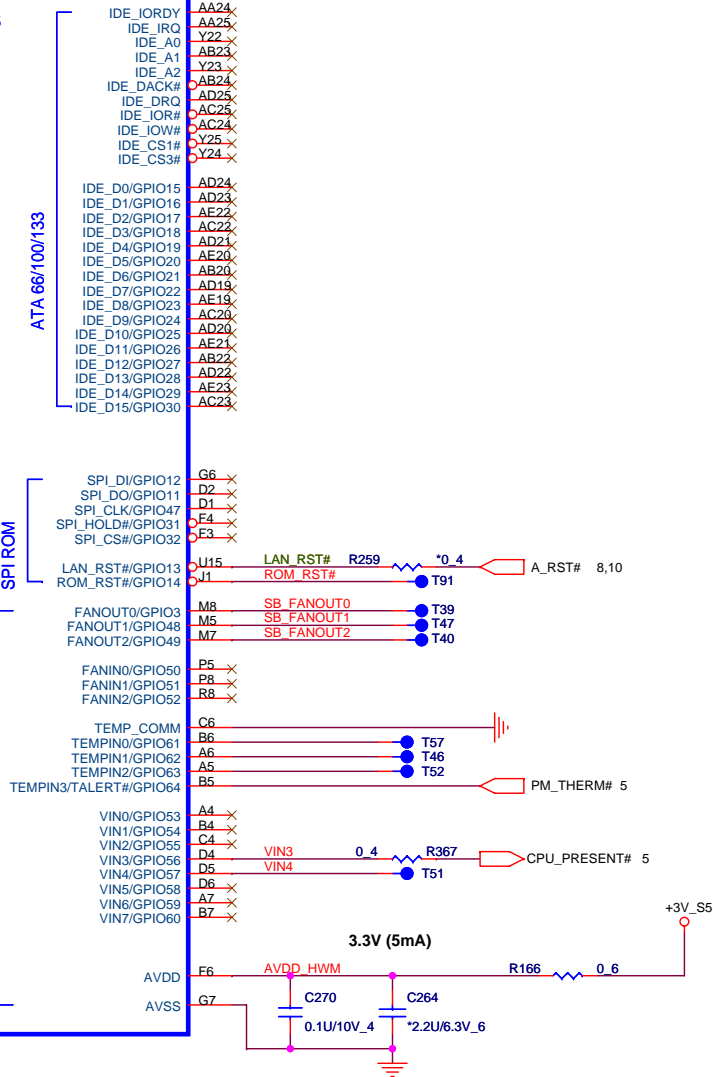
SB710
Part 2 of 5

SERIAL ATA

SPI ROM

HW MONITOR

ATA 66/100/133

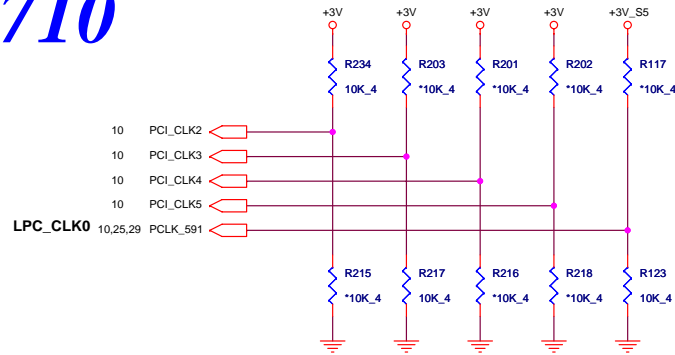


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Size	Document Number	Rev
	SB710-SATA/IDE/HWM/SPI 3/4	1A
Date:	Thursday, October 22, 2009	Sheet 12 of 42

Pin	Function	Pin	Function
1	T10	15	A15
2	U10	16	B15
3	U11	17	C14
4	U12	18	D9
5	V11	19	D11
6	V14	20	D13
7	W9	21	D14
8	Y9	22	D15
9	Y11	23	E15
10	Y14	24	F12
11	Y17	25	F14
12	A89	26	G9
13	AB11	27	H9
14	AB13	28	H17
15	AB15	29	J9
16	AB17	30	J11
17	A28	31	J12
18	ADB	32	J14
19	AE8	33	J15
20		34	K10
21		35	K12
22		36	K14
23		37	K15
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130		144	

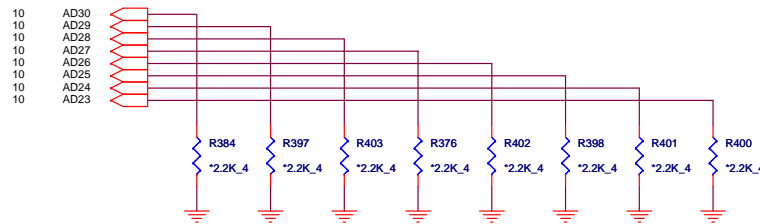


REQUIRED STRAPS

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0
PULL HIGH	BOOTFAIL TIMER ENABLED DEFAULT	USE DEBUG STRAPS	RESERVED	RESERVED	EC ENABLED
PULL LOW	BOOTFAIL TIMER DISABLED	IGNORE DEBUG STRAPS DEFAULT			EC DISABLED DEFAULT

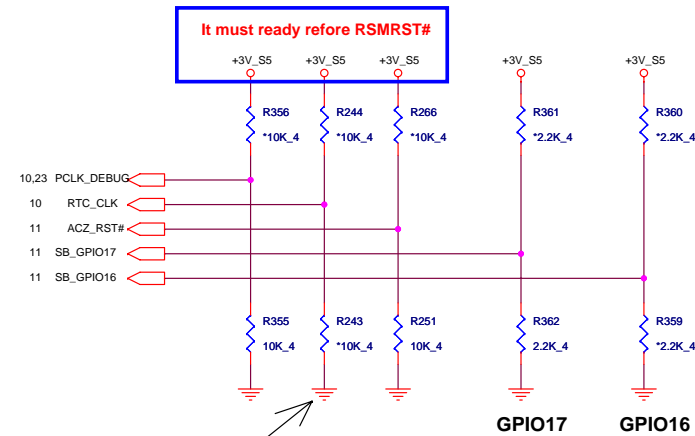
DEBUG STRAPS

SB710 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



REQUIRED STRAPS

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD29	PCI_AD30
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED		
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS		RESERVED	RESERVED

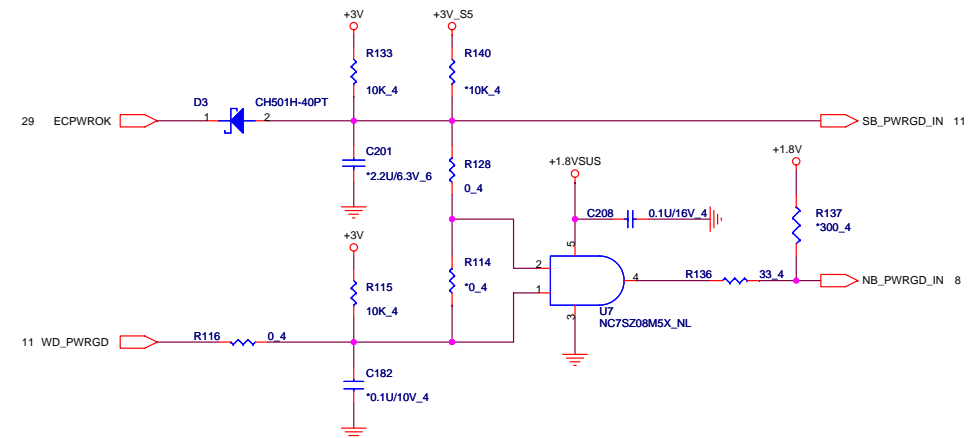


NOTE: SB710 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

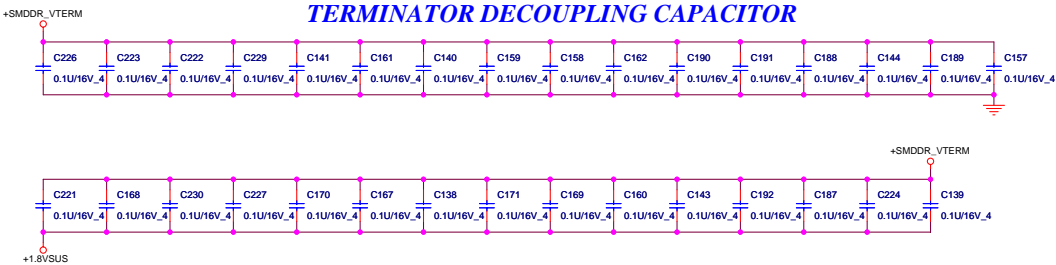
NOTE: SB710 HAS INTERNAL 15K PULL UP RESISTOR FOR SB_GPIO16, SB_GPIO17.

	LPC_CLK1	RTC_CLK	ACZ_RST#	GP17	GP16
PULL HIGH	CLKGEN ENABLED	INTERNAL RTC DEFAULT	ENABLE PCI MEM BOOT	ROM TYPE: H, H = Reserved	
PULL LOW	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI MEM BOOT DEFAULT	H, L = SPI ROM L, H = LPC ROM L, L = FWB ROM	DEFAULT

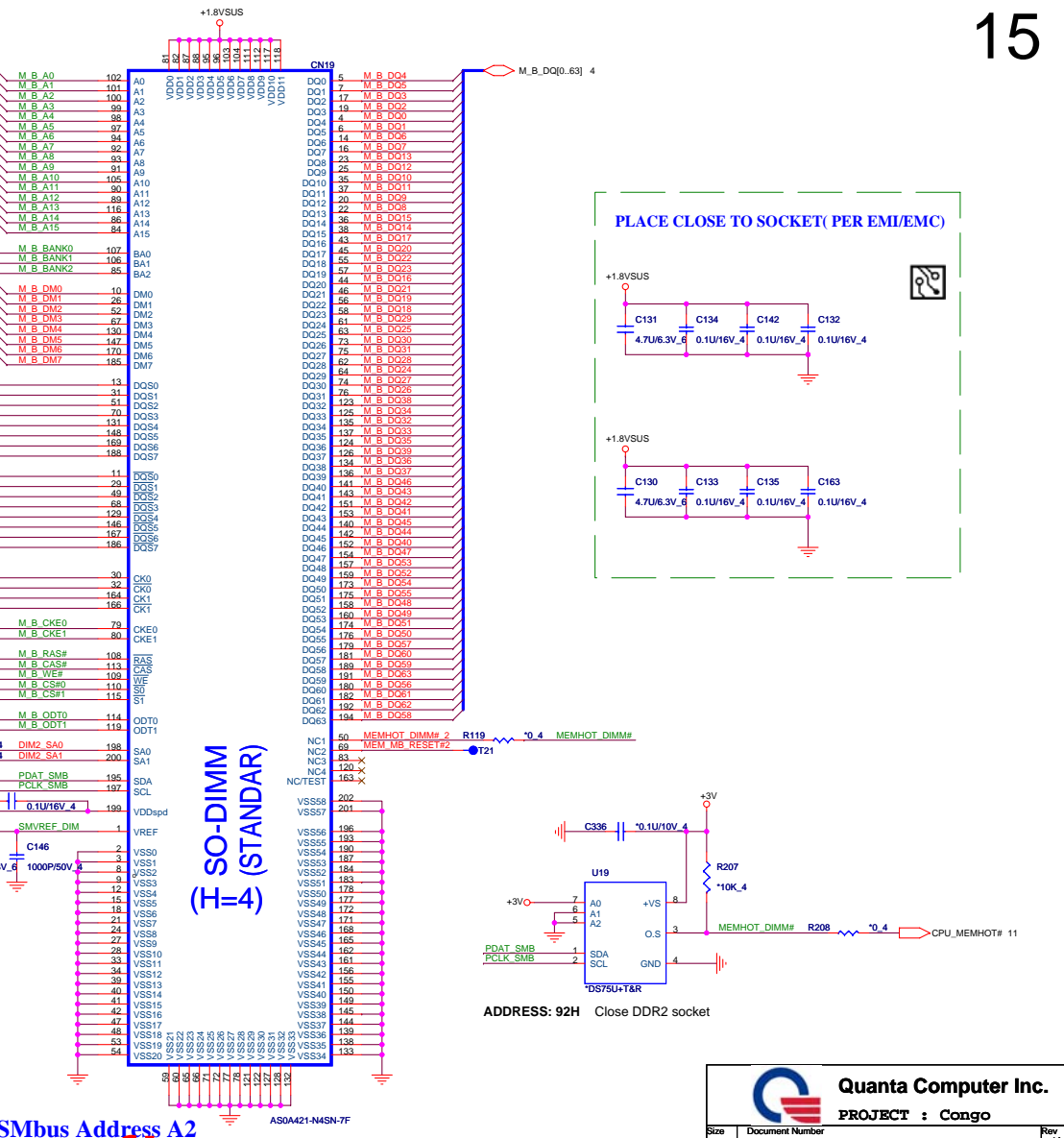
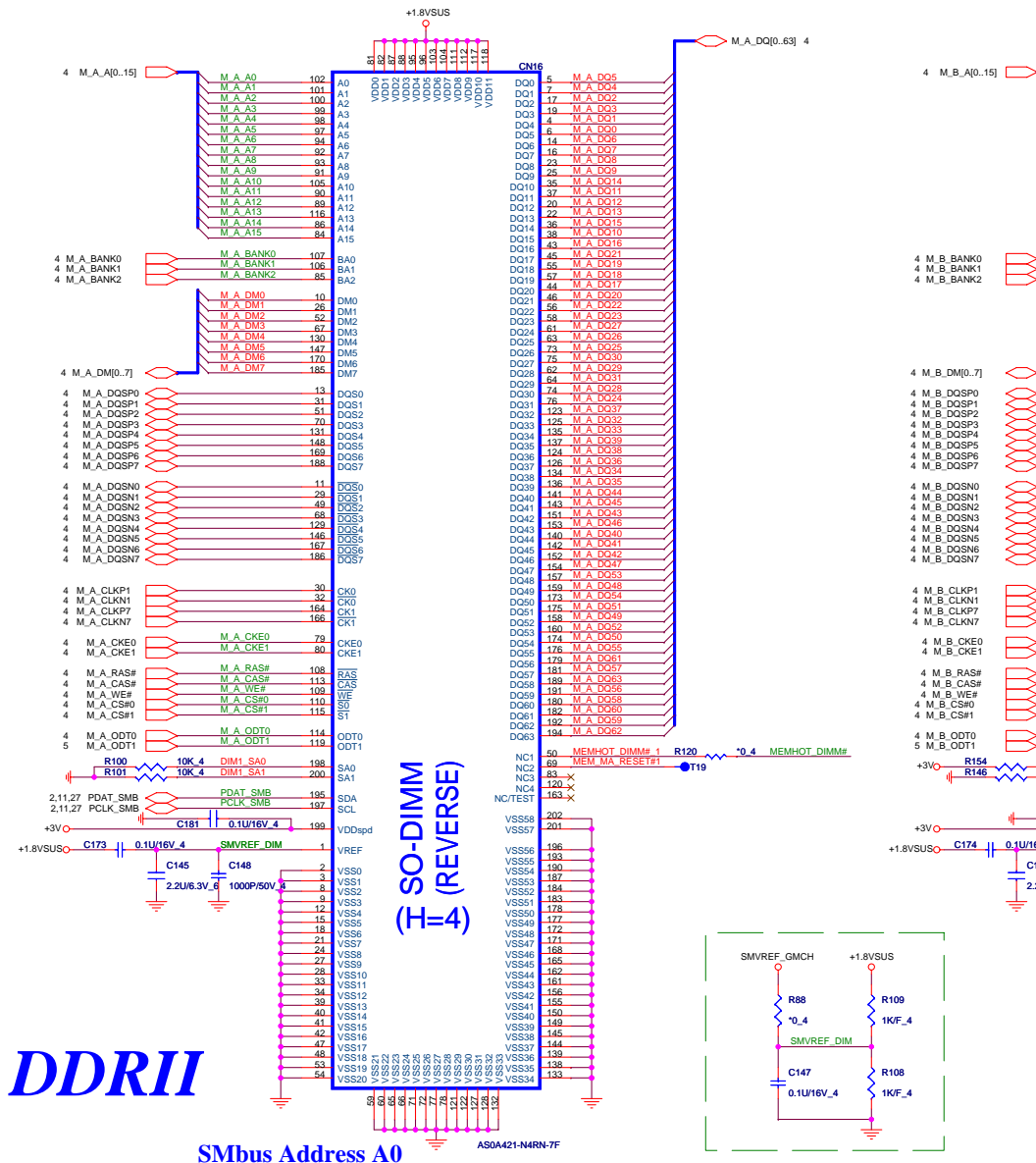
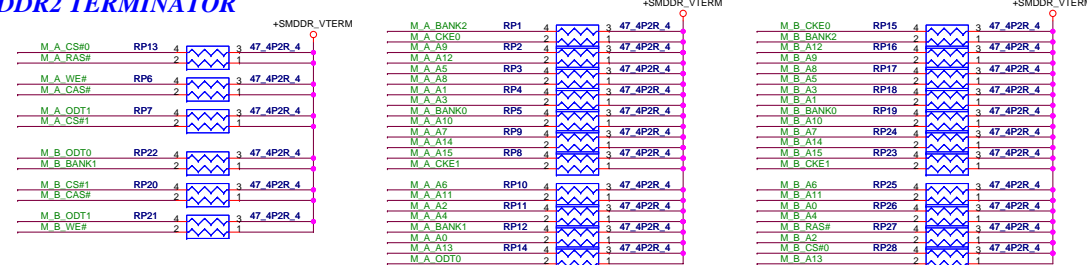
NB/SB POWER GOOD CIRCUIT



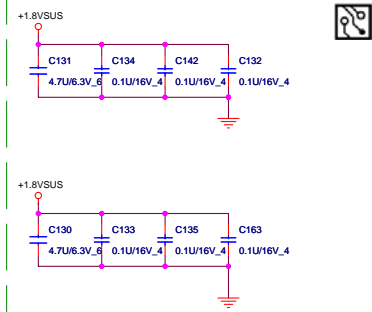
TERMINATOR DECOUPLING CAPACITOR



DDR2 TERMINATOR



PLACE CLOSE TO SOCKET (PER EMI/EMC)



DDR2

Smbus Address A0

(H=4)

(H=4)

Smbus Address A2

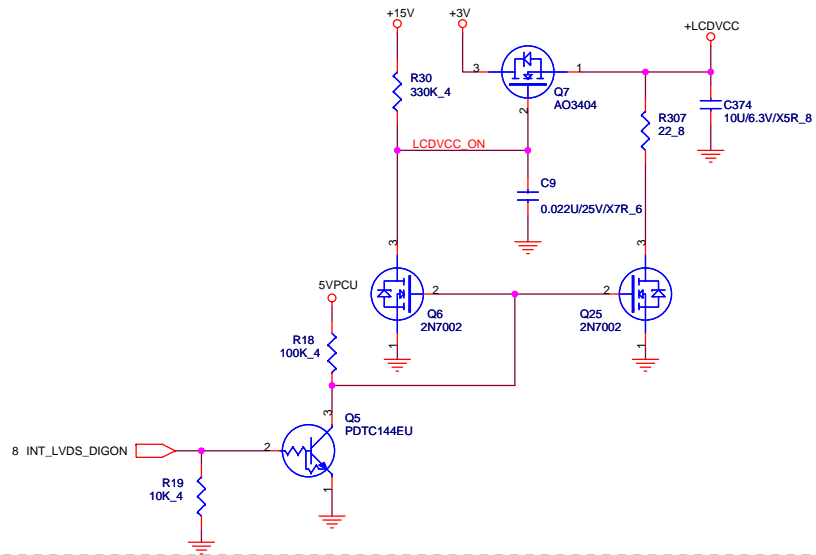
(H=4)

(H=4)

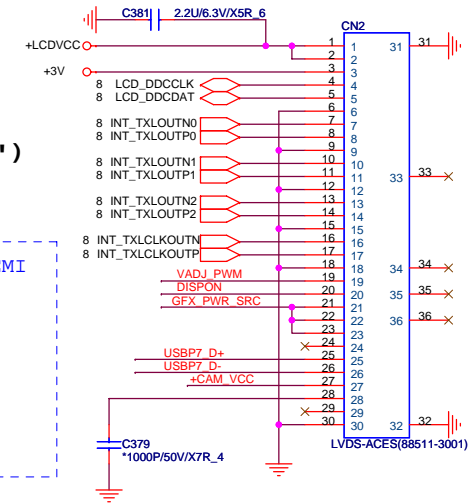
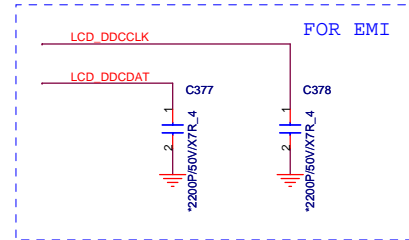
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Size Document Number
DDR2 SODIMMS: A/B CHANNEL
Date: Thursday, October 22, 2009 Sheet 15 of 42

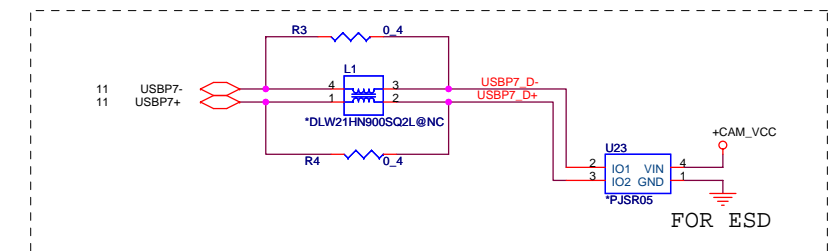
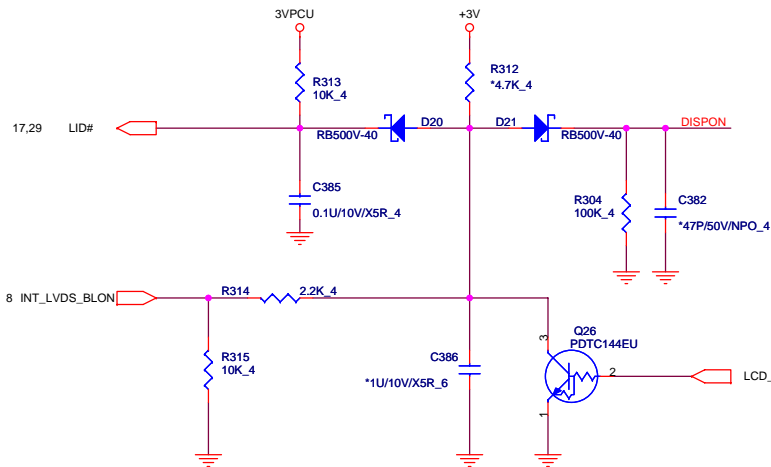
LCDVCC



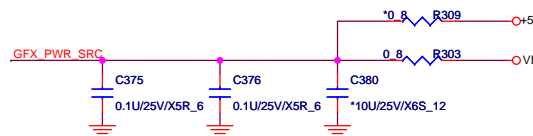
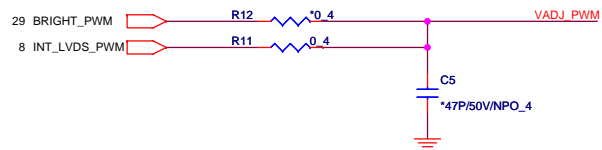
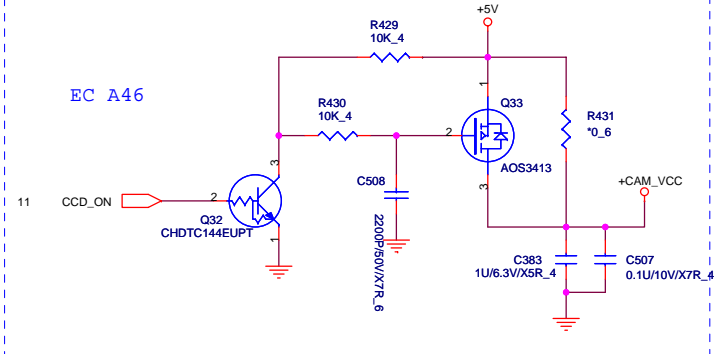
LVDS (11.6")
(1024x600,
1366x768)

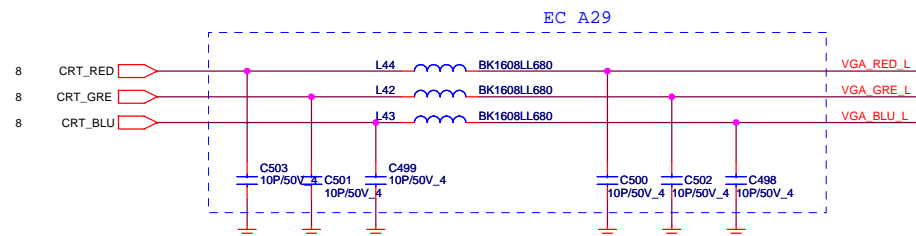
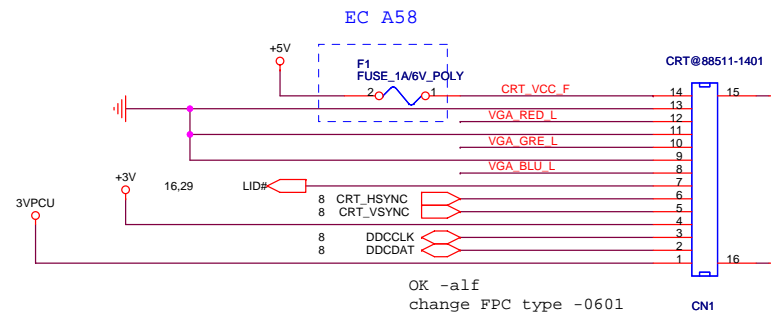


Back light

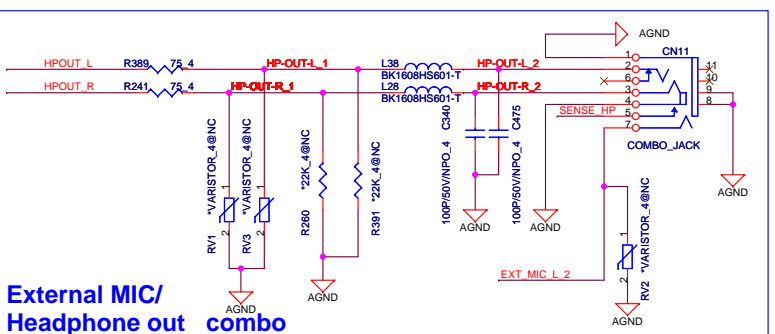
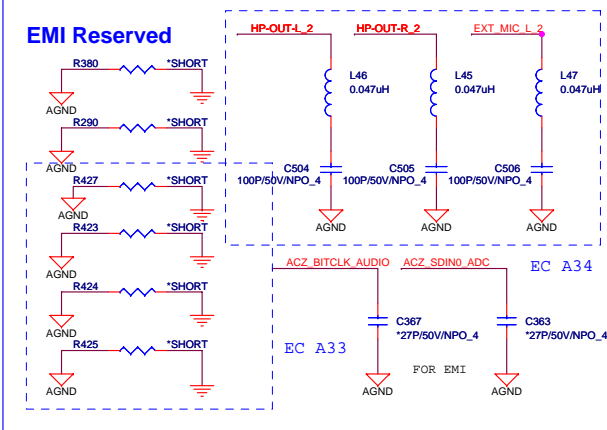
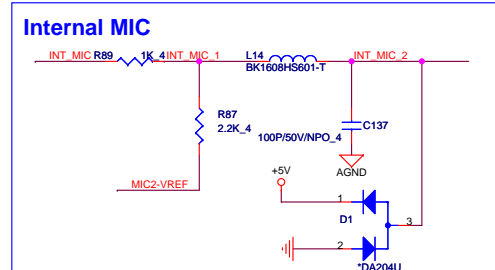
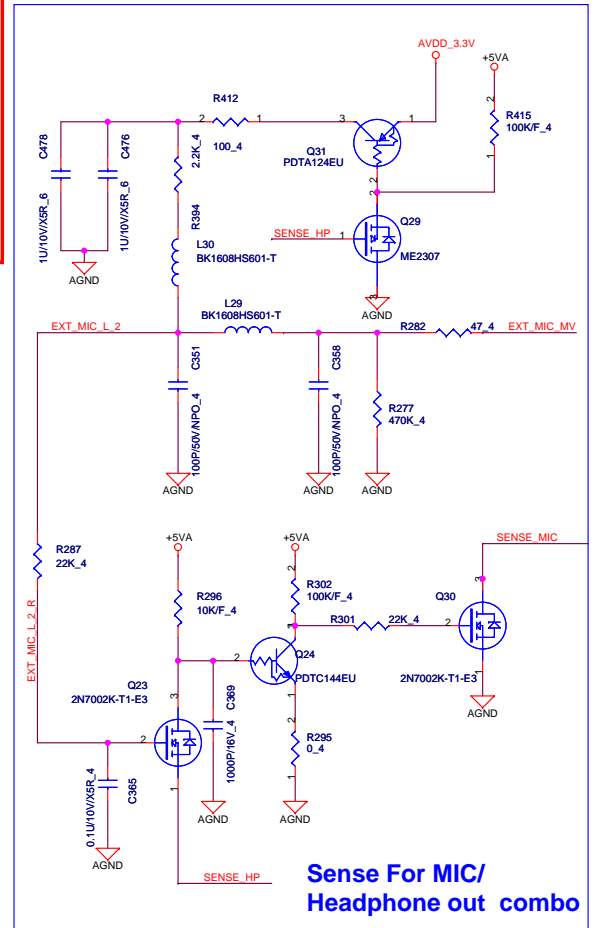


CAMERA VCC Control

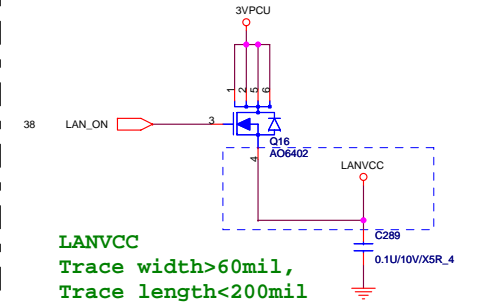




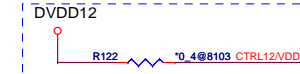
Layout Note: Path from +5V to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms). Place bypass caps very close to device.



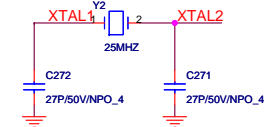
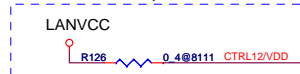
LANVCC



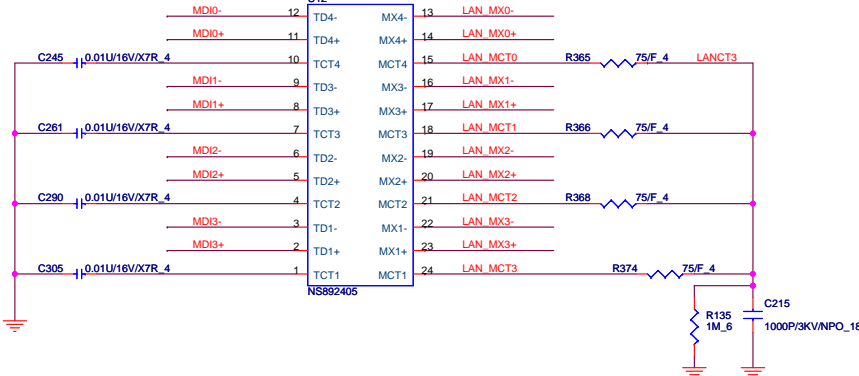
For RTL8102EL/8103EL, use this block.



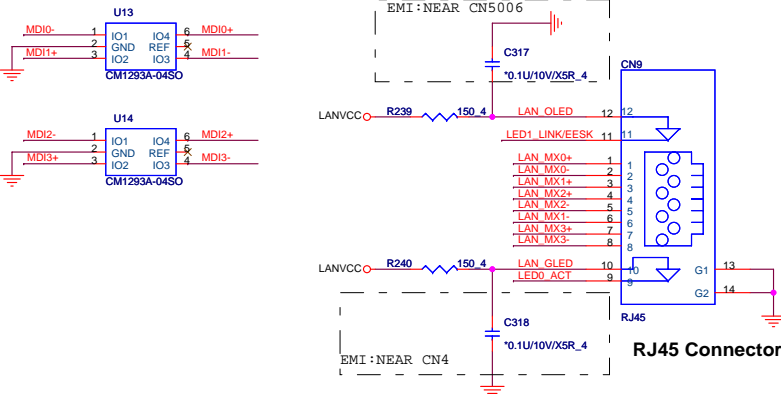
For RTL8111DL, use this block



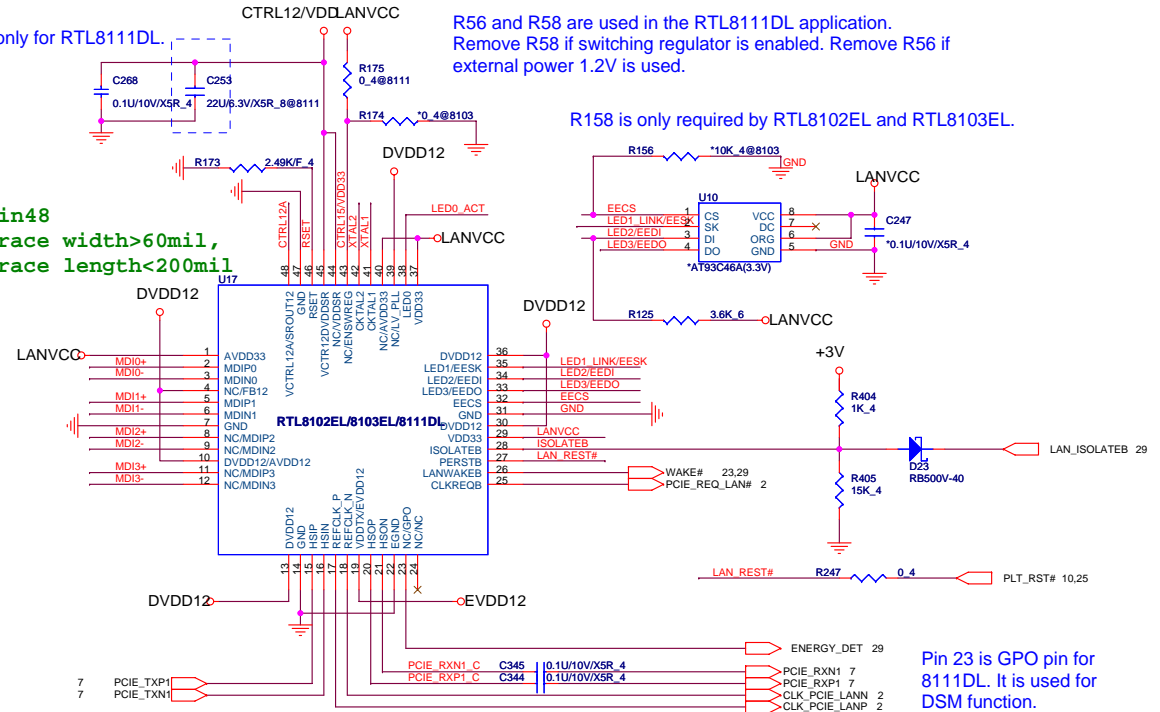
Transformer



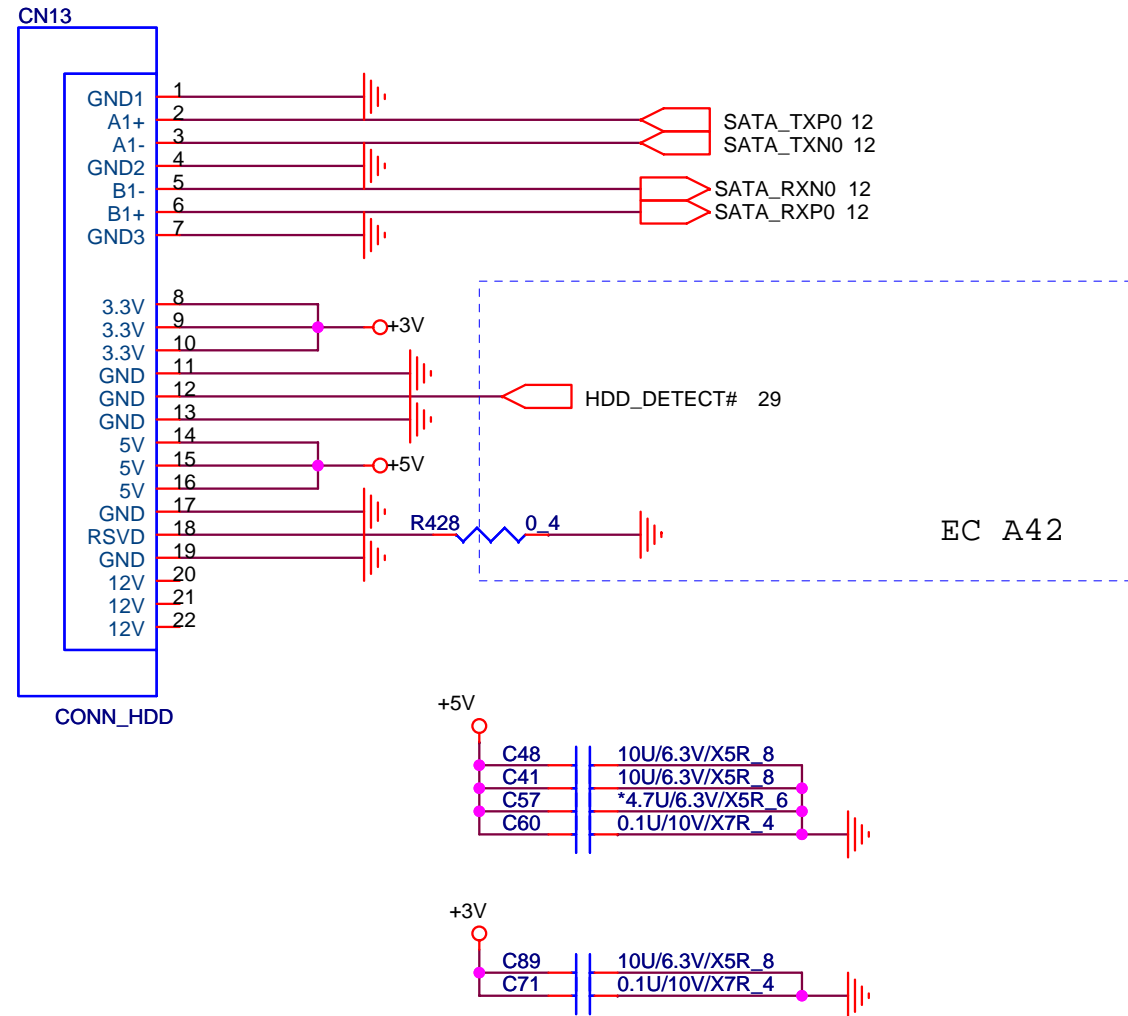
RJ45 Connector



C70 is only for RTL8111DL

Pin48
Trace width>60mil,
Trace length<200mil

DC Current rating: 0.5 A



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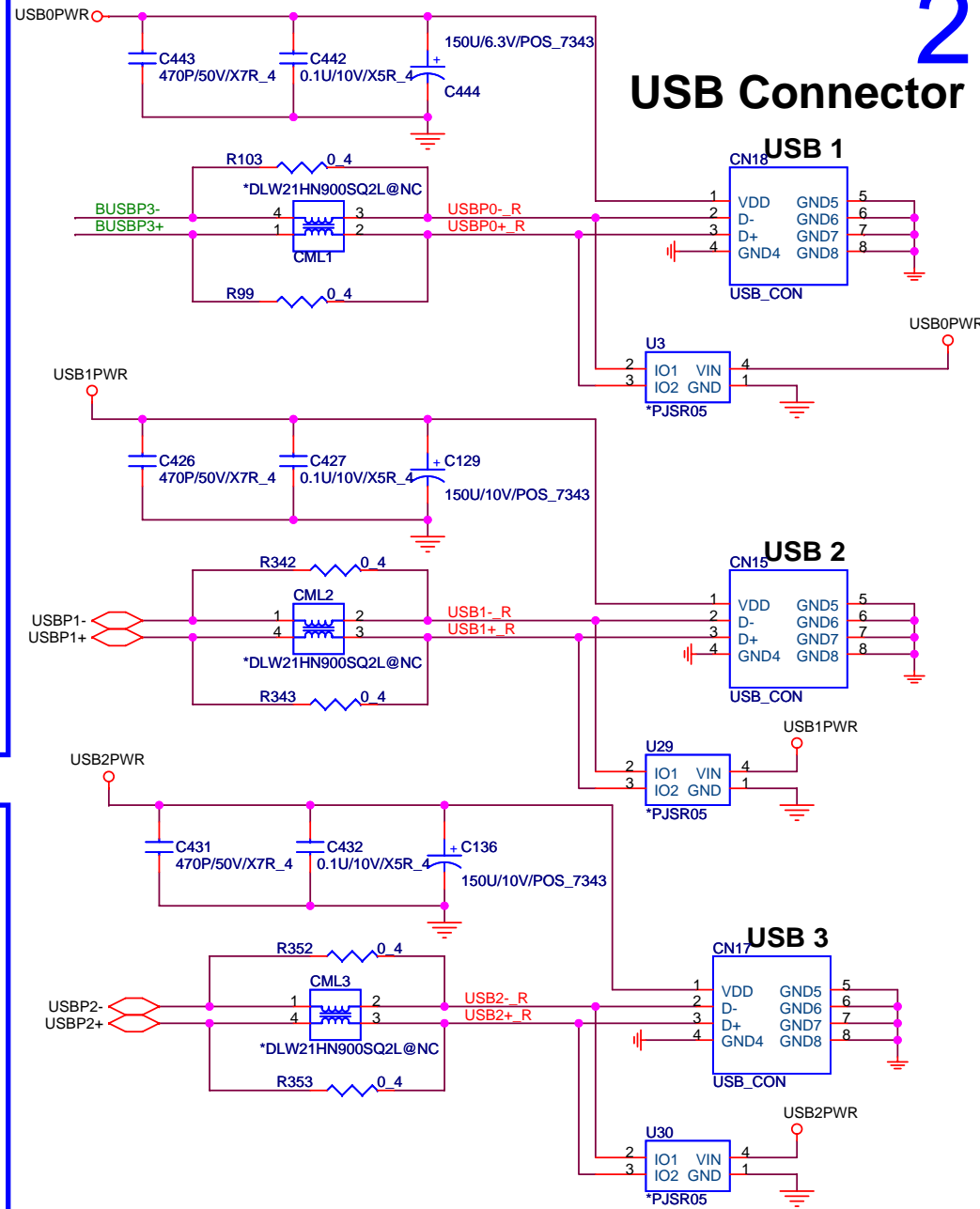
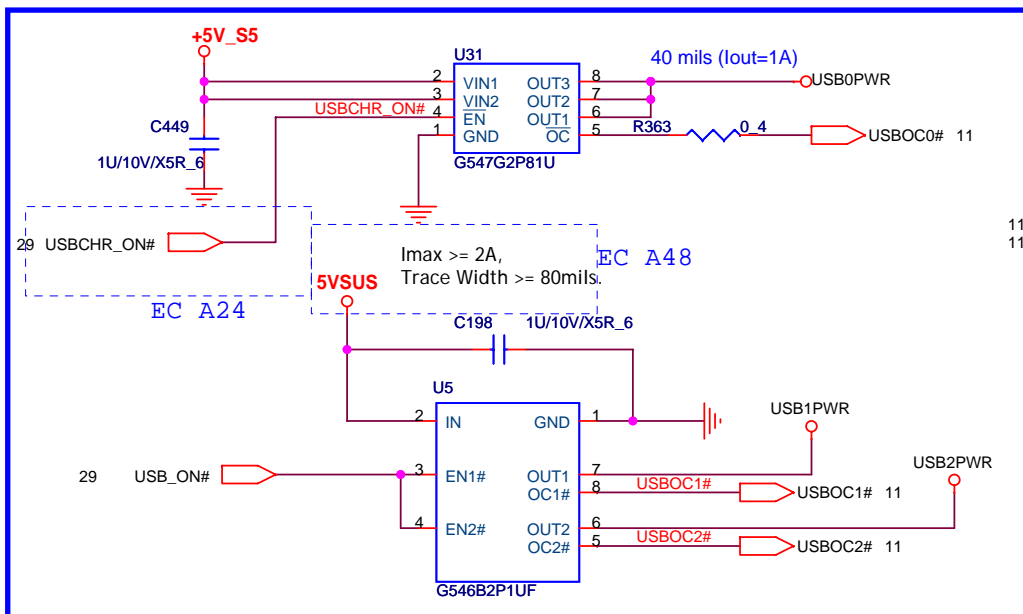
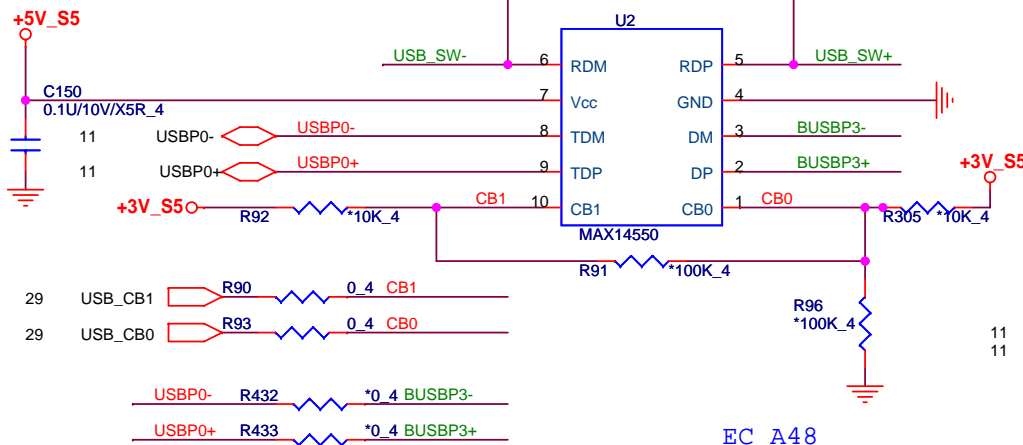
PROJECT : Congo

Size	Document Number	Rev
	SATA	1A
Date	Thursday, October 22, 2009	Sheet 20 of 42

USB SLEEP CHARGE (NEW)

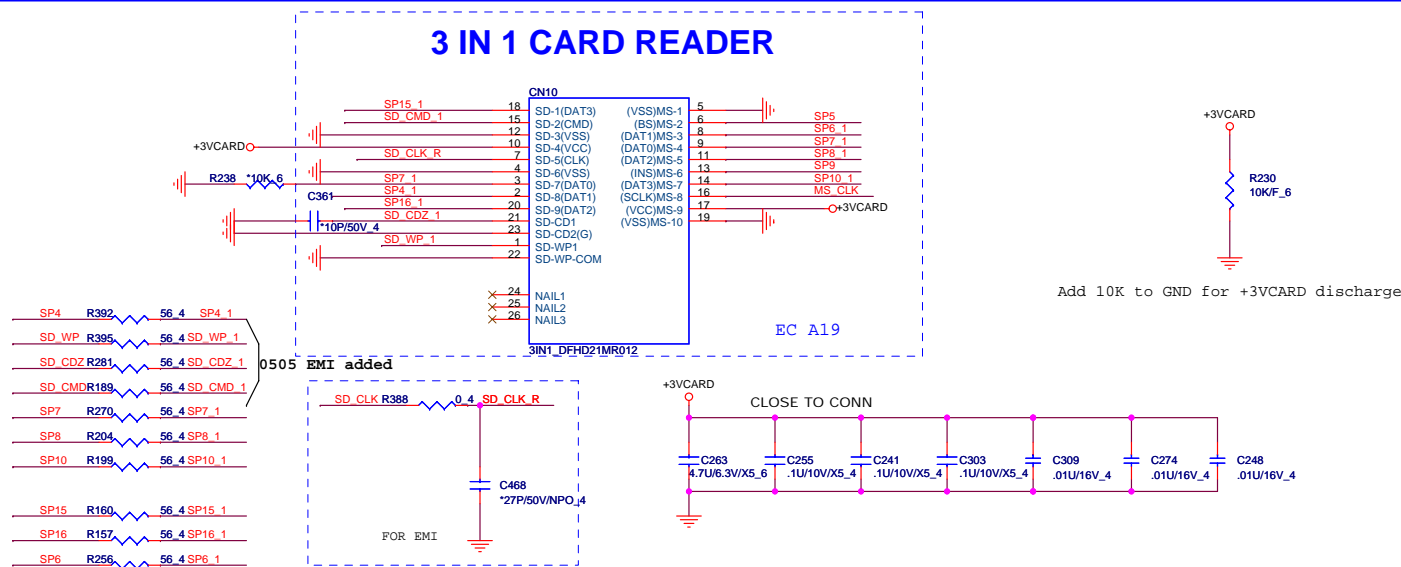
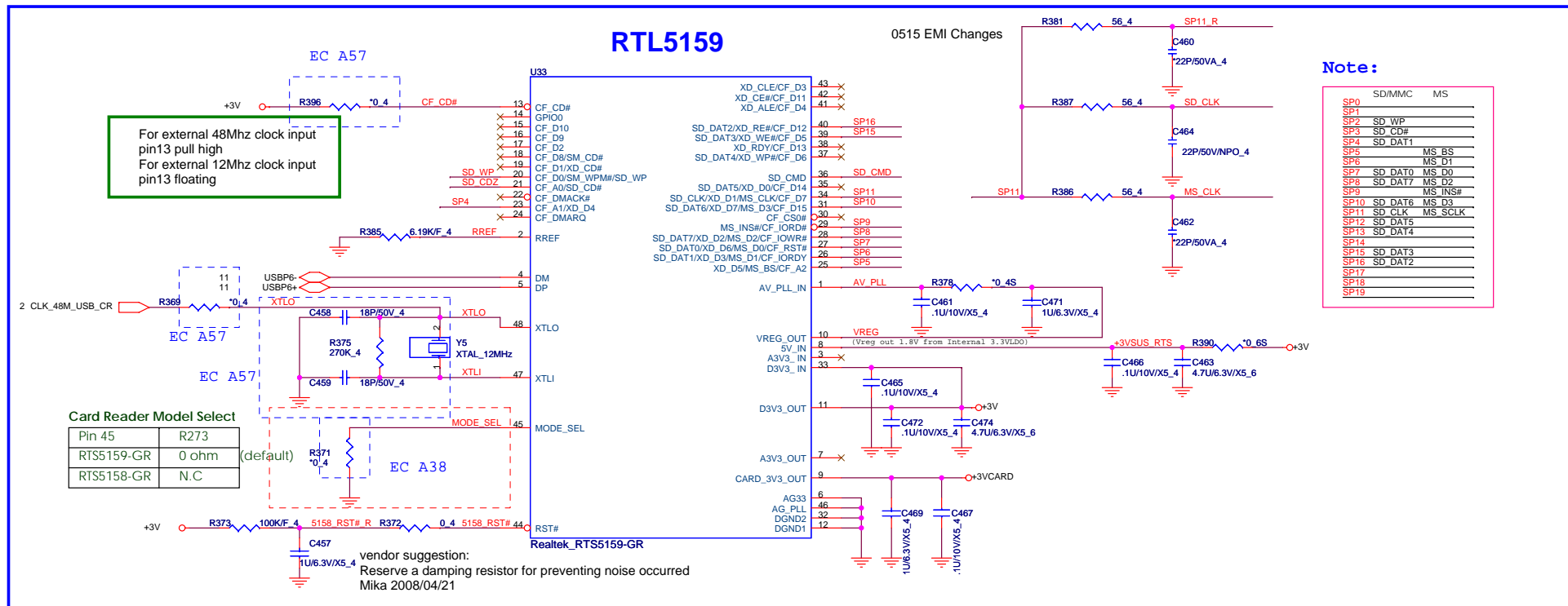
CB0/CB1	Function	Int./Ext. R
0 0	S5 auto detect	Use Int.R
0 1	Blackberry(choice)	NC
1 0	iPod/iPhone(choice)	Use Ext. R
1 1	S0 auto detect	NC

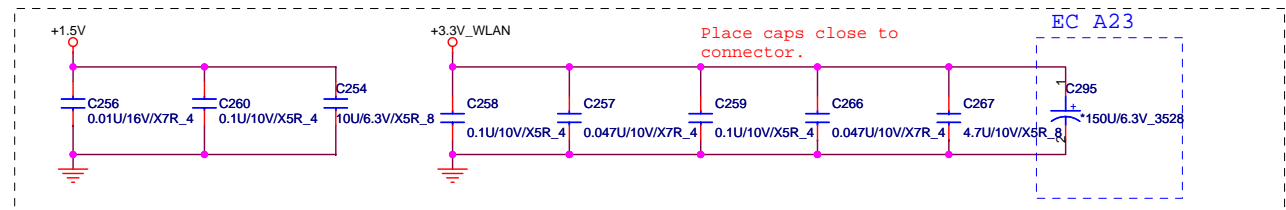
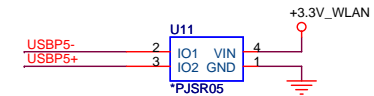
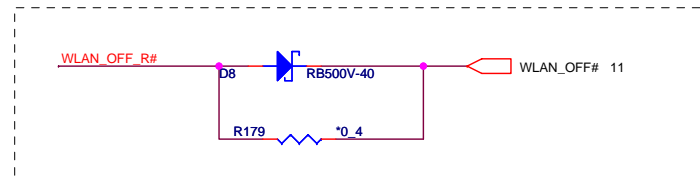
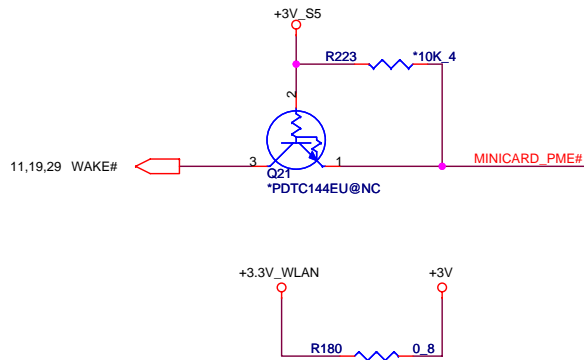
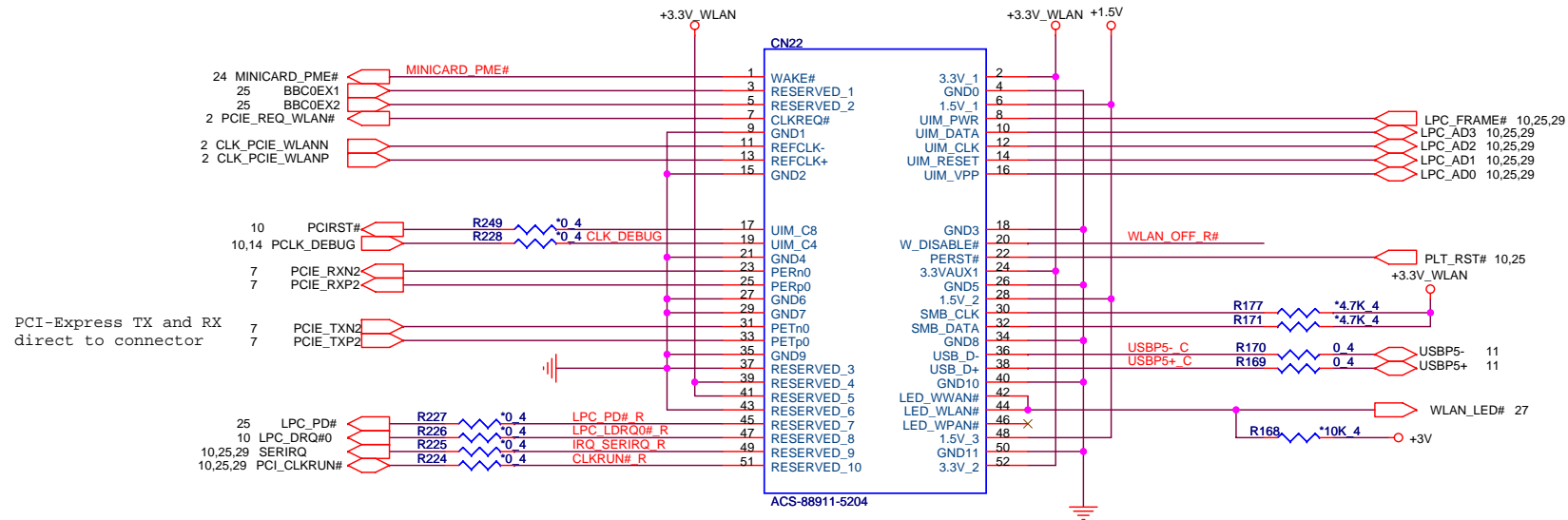
Sleep charger notice



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PROJECT : Congo

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	USB x 3	1A
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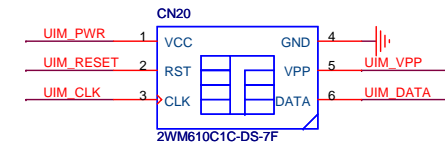


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PROJECT : Congo

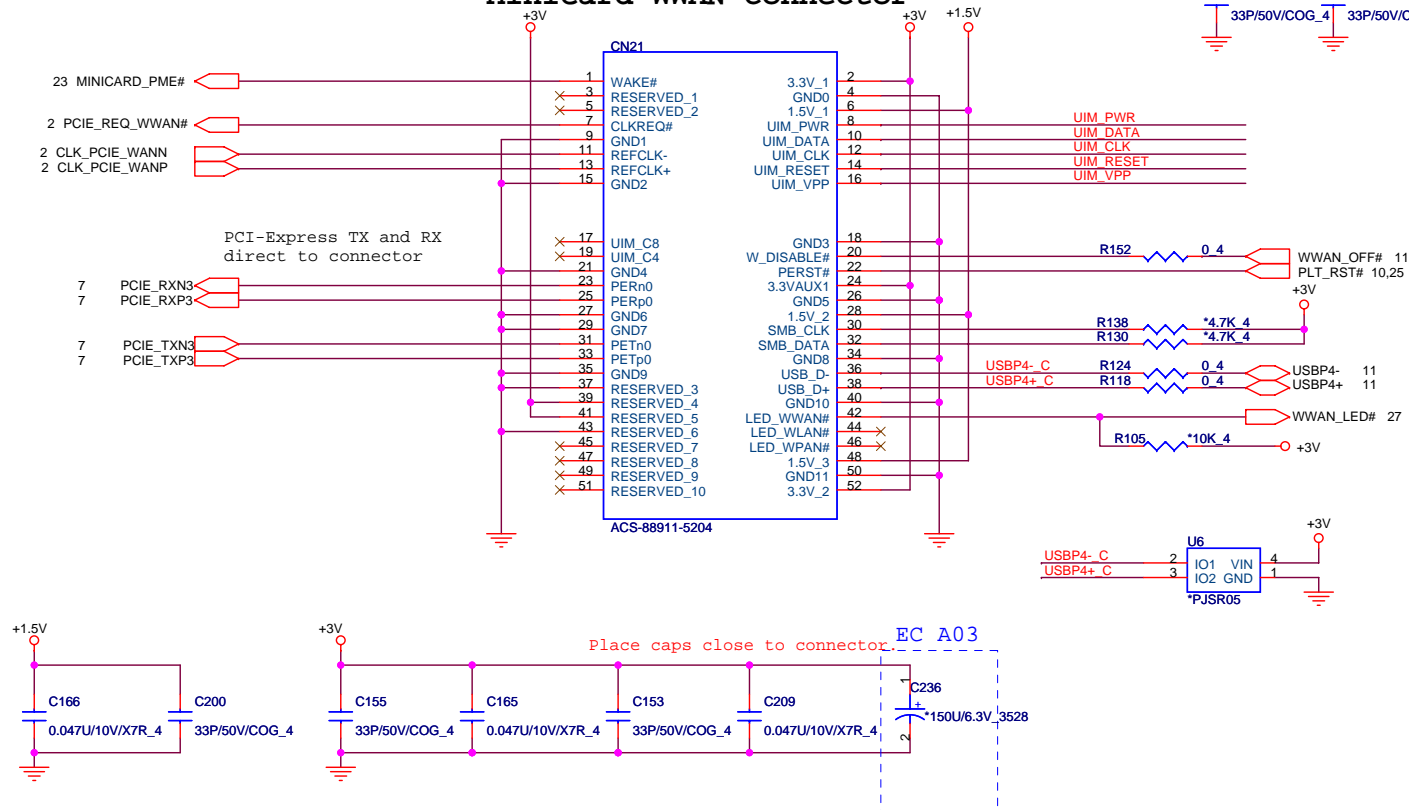
Size	Document Number	Rev
	WLAN	1A
Date:	Thursday, October 22, 2009	Sheet 23 of 42

SIM Card CONN



Layout Note:
UIM_RESET, UIM_CLK, UIM_DATA routing as short as possible

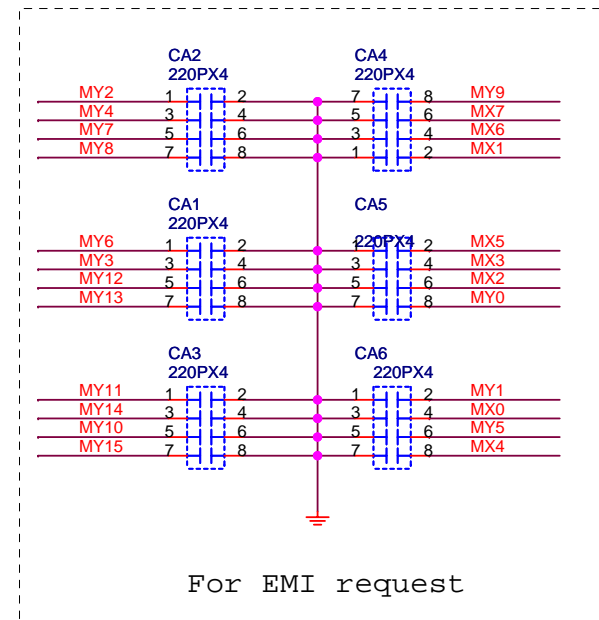
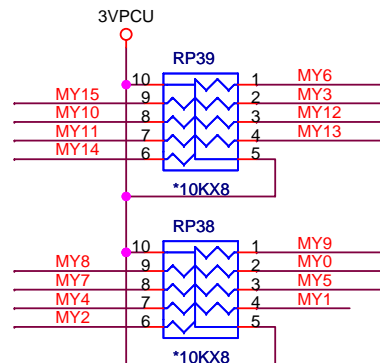
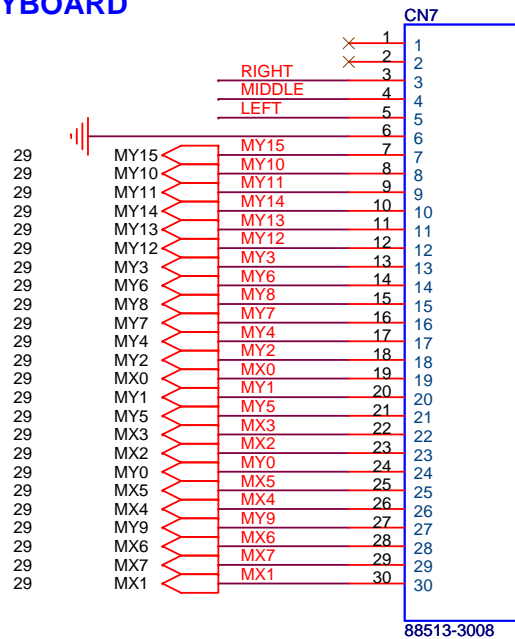
MiniCard WWAN connector



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PROJECT : Congo

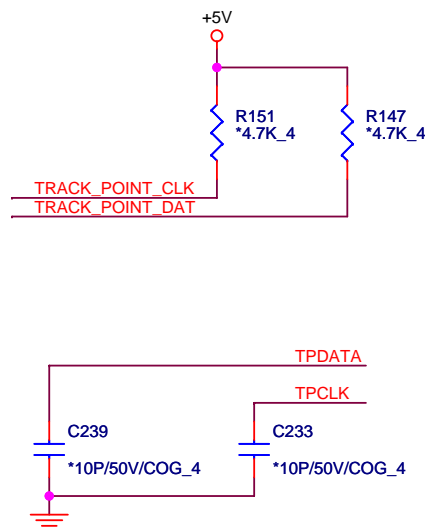
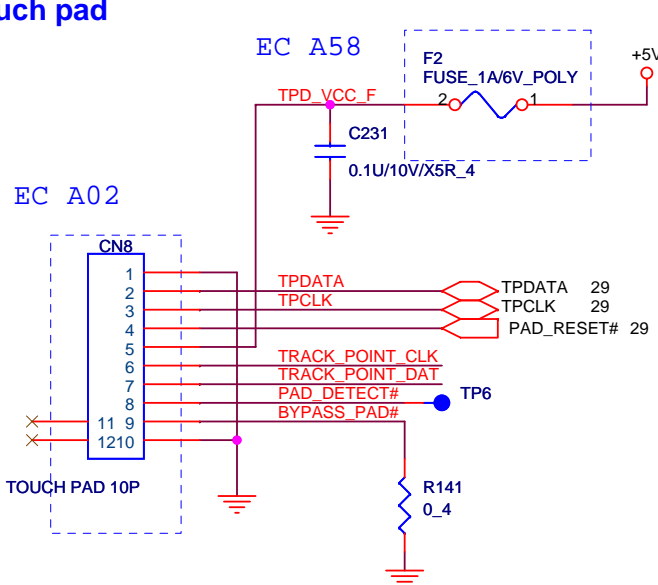
Size	Document Number	Rev
	WWAN	1A
Date:	Thursday, October 22, 2009	Sheet 24 of 42

KEYBOARD

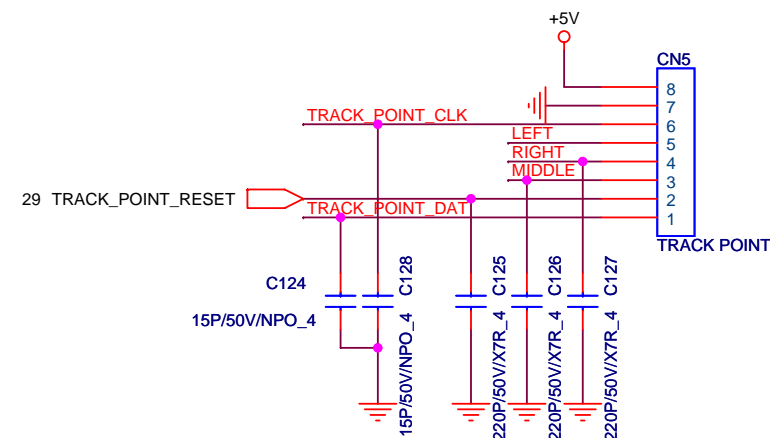


26

Touch pad

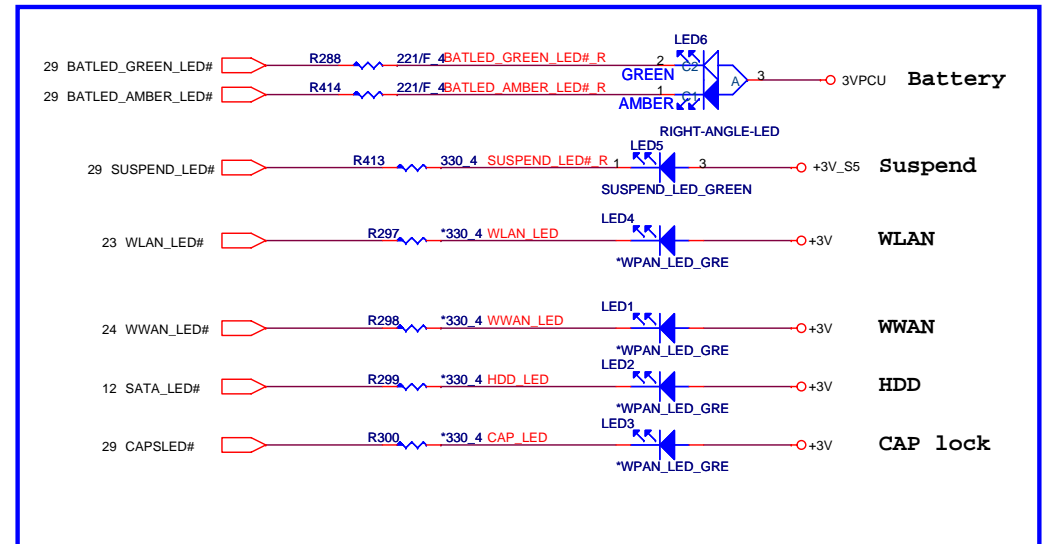
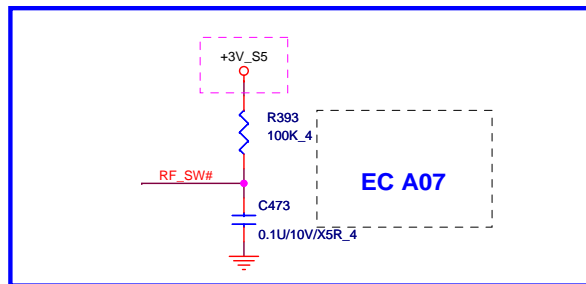


TRACK POINT

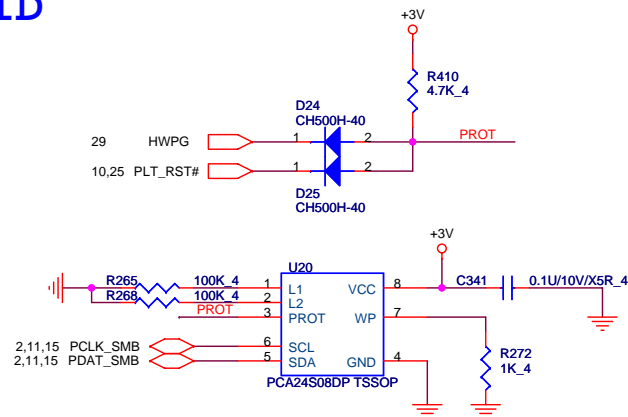


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PROJECT : Congo

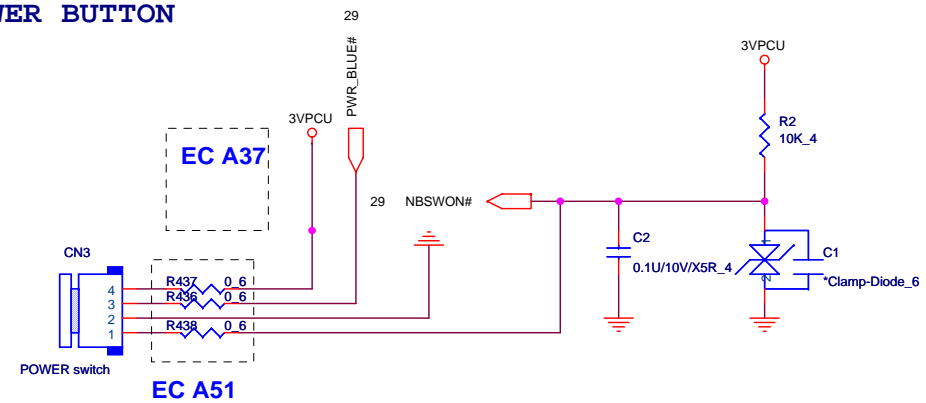
Size	Document Number	KB/TP	Rev 1A
Date:	Thursday, October 22, 2009	Sheet 26 of 42	



RFID



POWER BUTTON



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PROJECT : Congo

SW/LED/RFID_EEPROM

Size Document Number

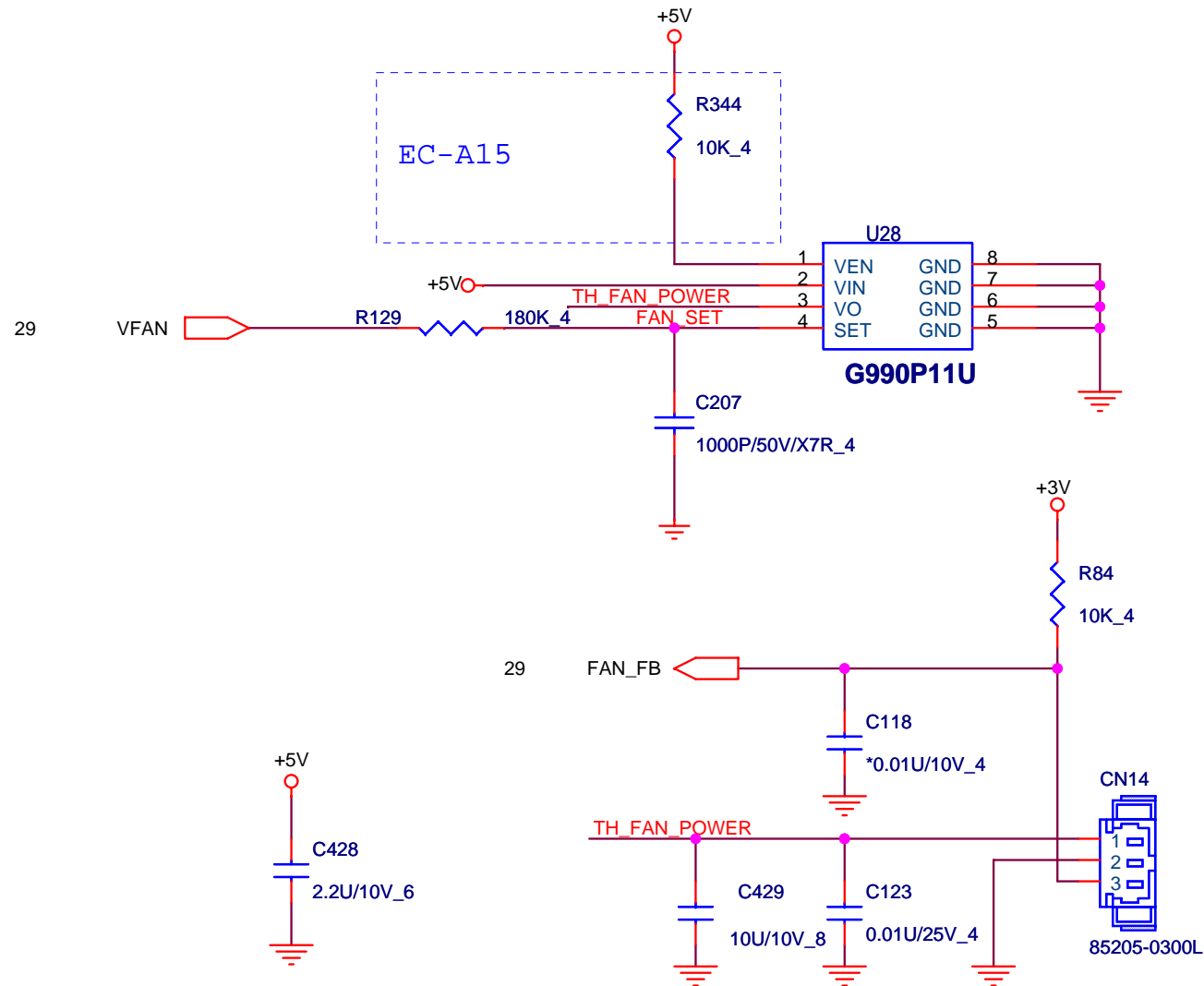
Date: Thursday, October 22, 2009

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Rev 1A

CPU FAN

FANPWR = 1.6*VSET



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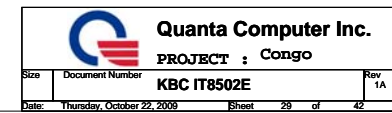
PROJECT : Congo

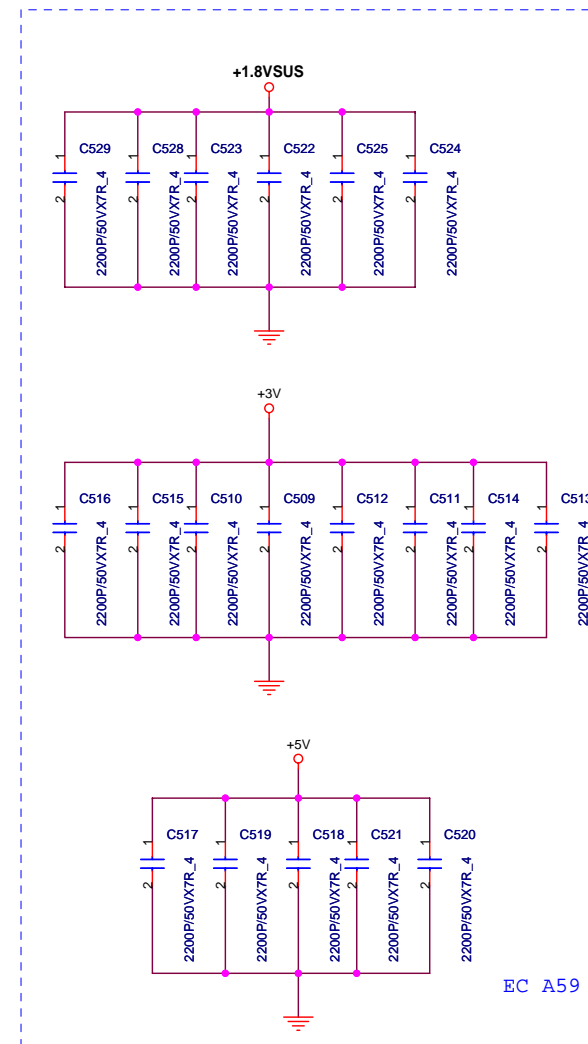
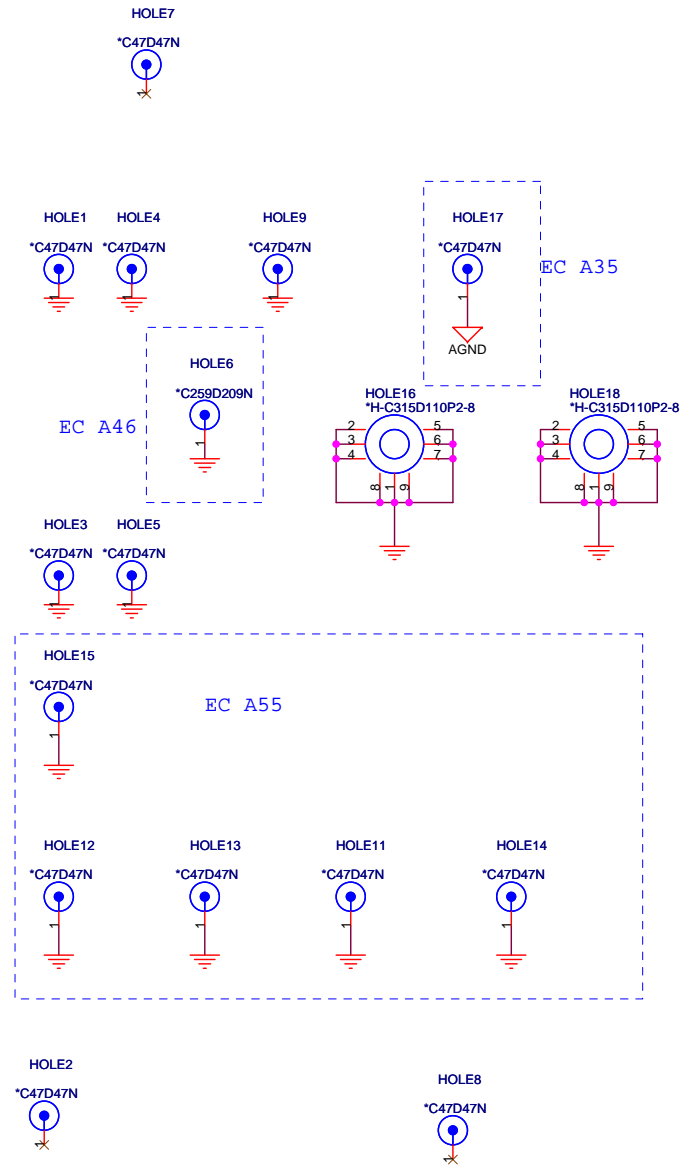
FAN/Thermal

Rev
1A

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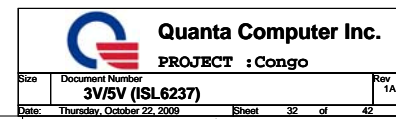
Quanta Computer Inc.

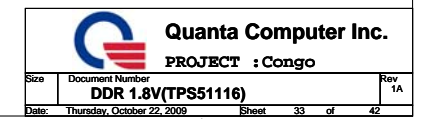
PROJECT : Congo

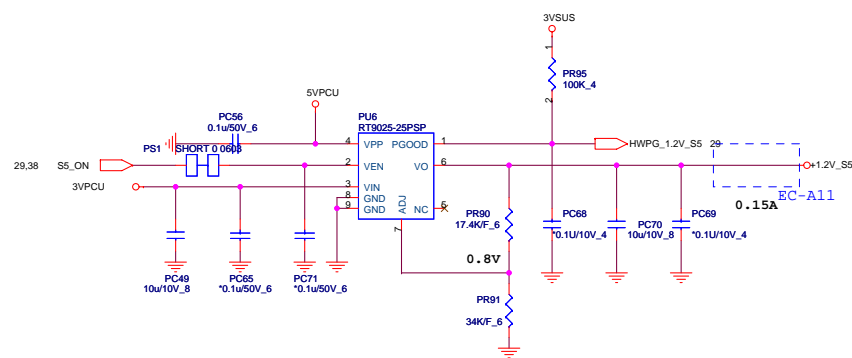
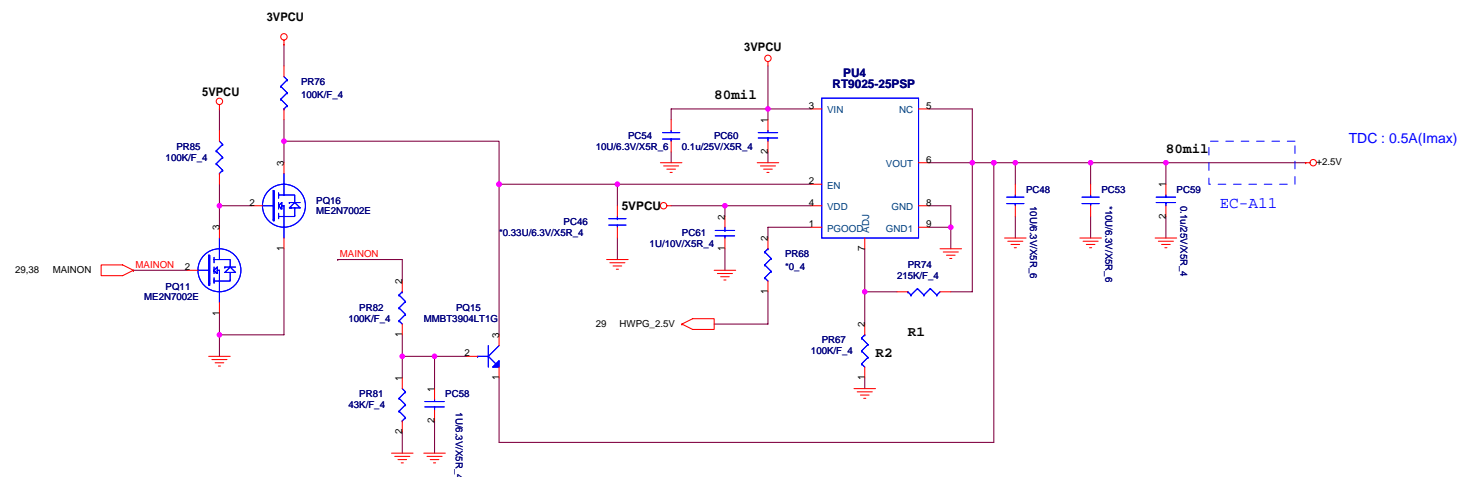
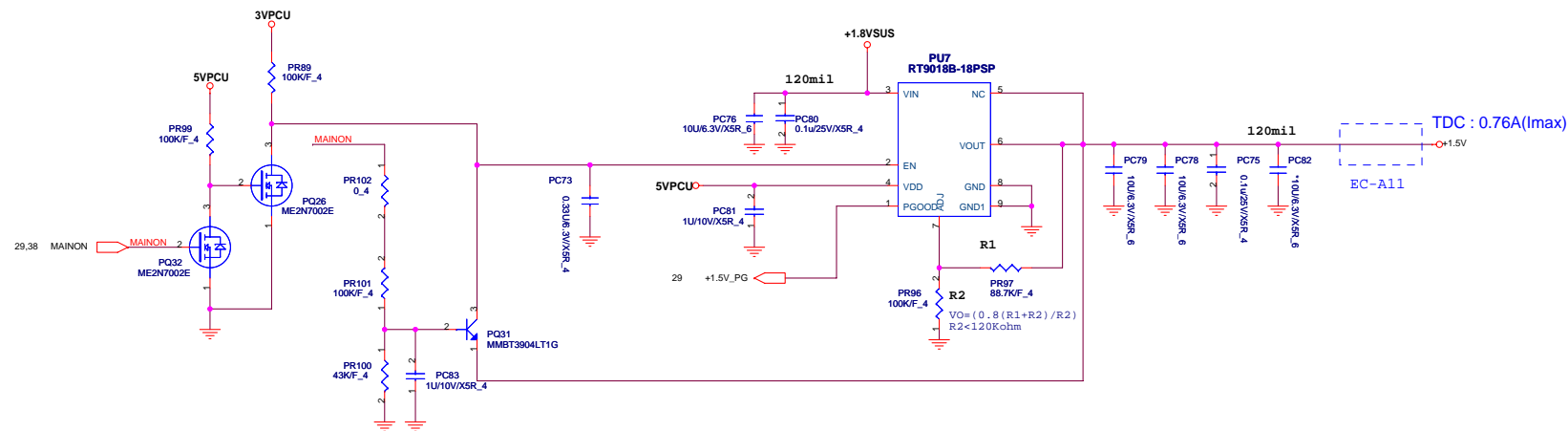
Screw Hole/EMI

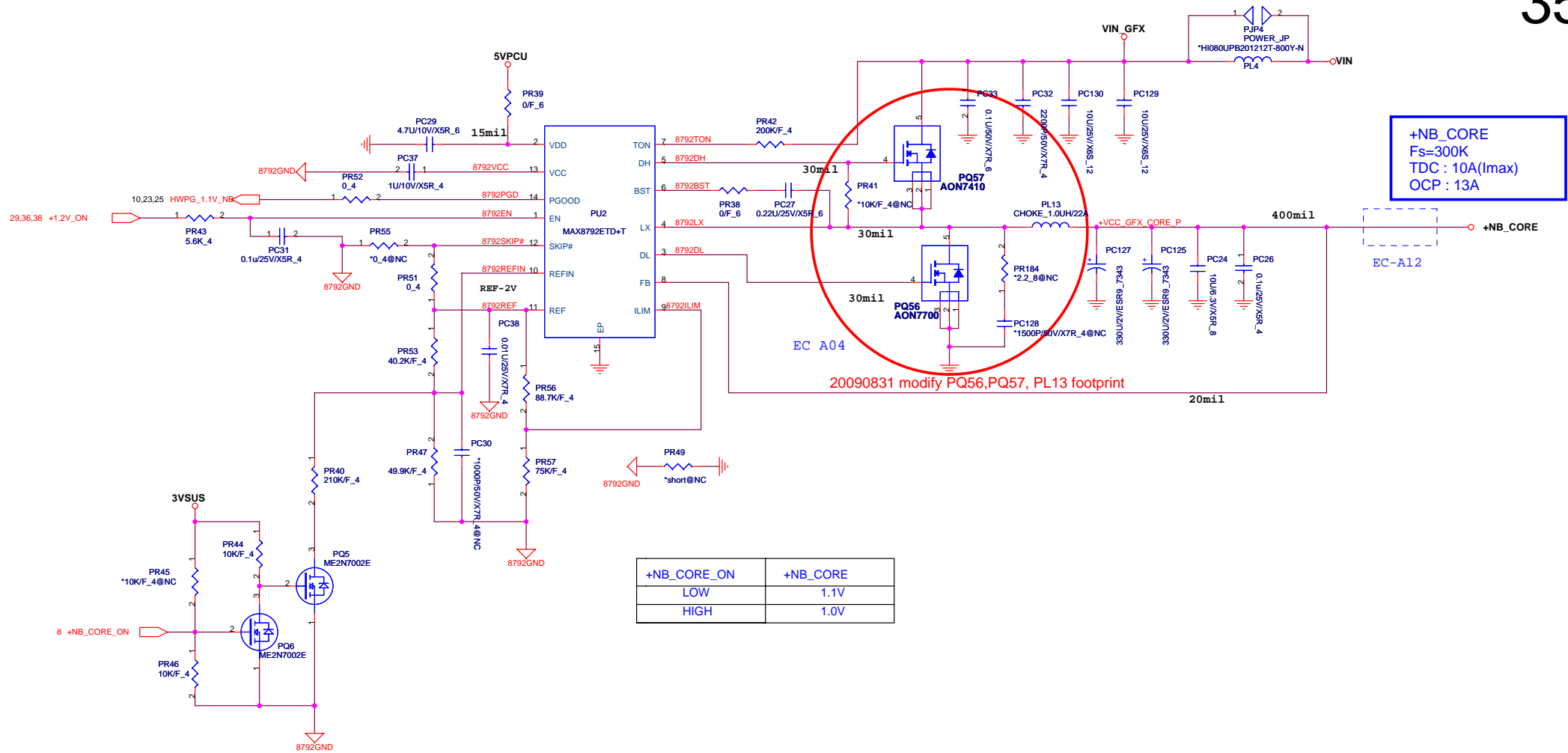
Size	Document Number	Rev
		1A
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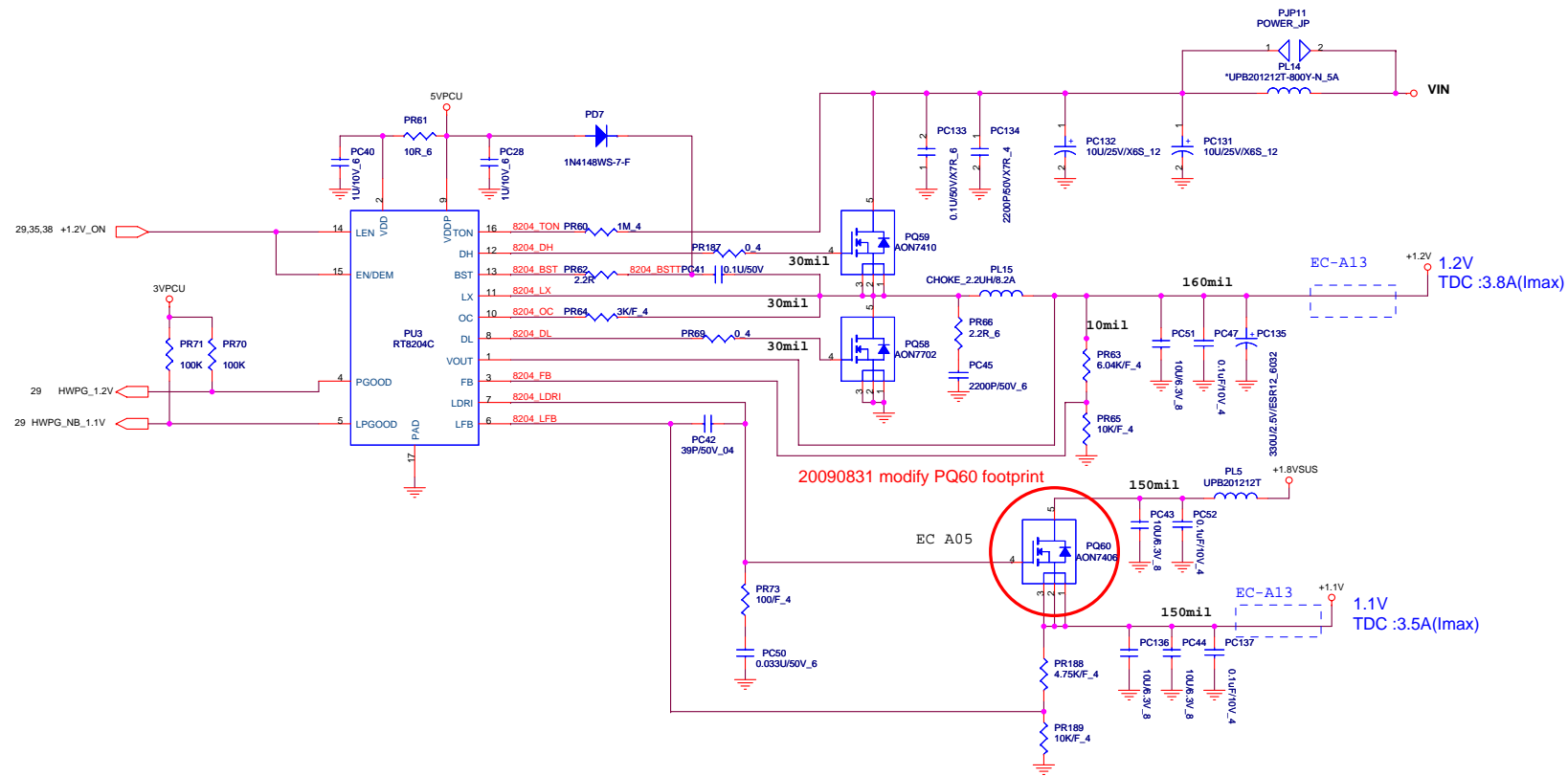




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PROJECT : Congo

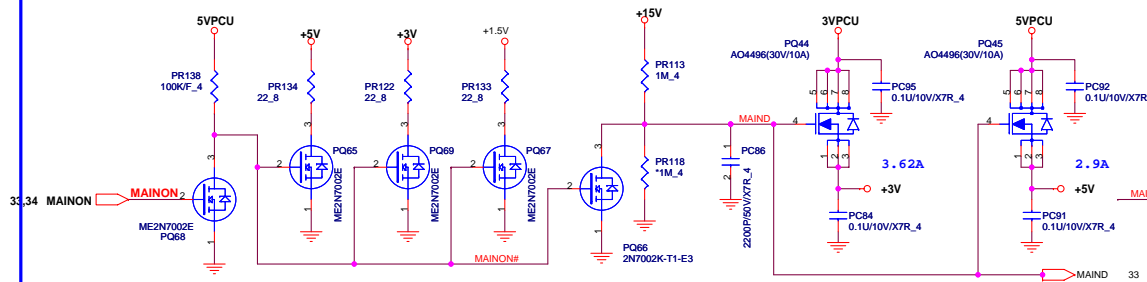
Size	Document Number	Rev
	+NB_CORE (MAX8792)	1A
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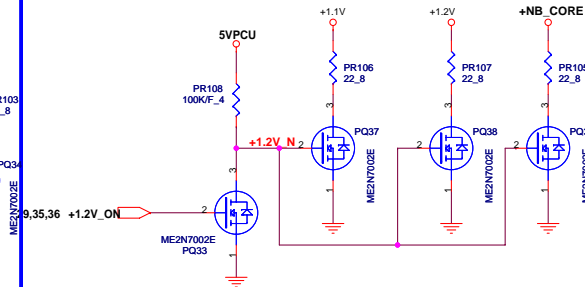


DISCHARGE

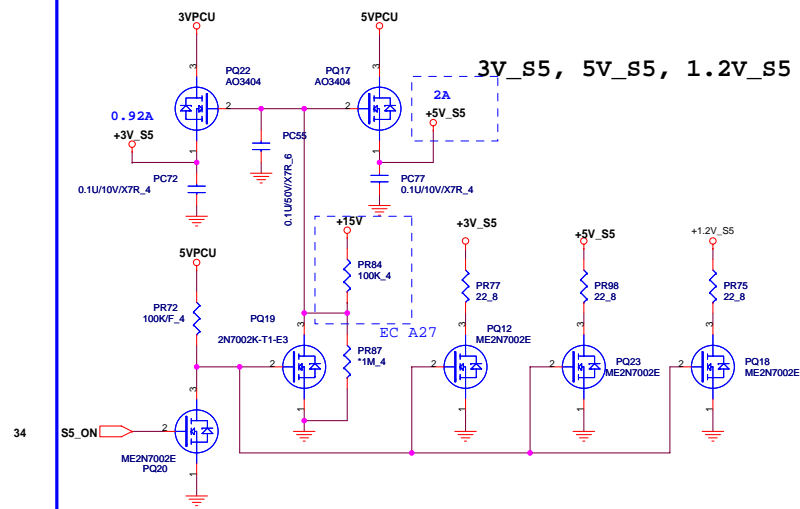
+3V, +5V, +2.5V, +1.5V



+1.1V, +1.2V, +NB_CORE

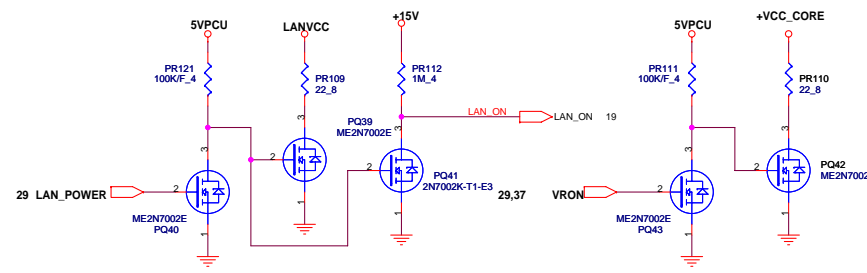


3V_S5, 5V_S5, 1.2V_S5

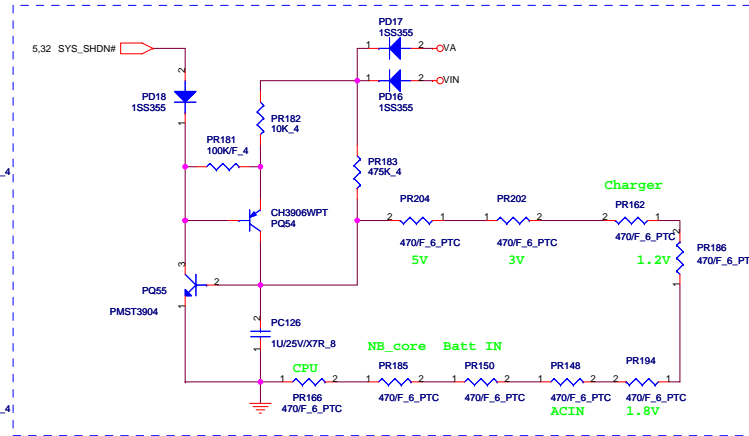
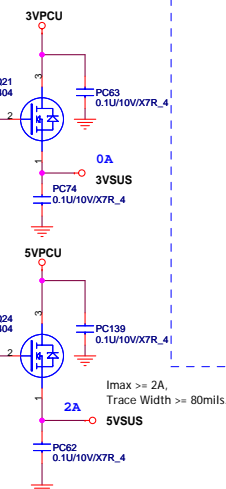
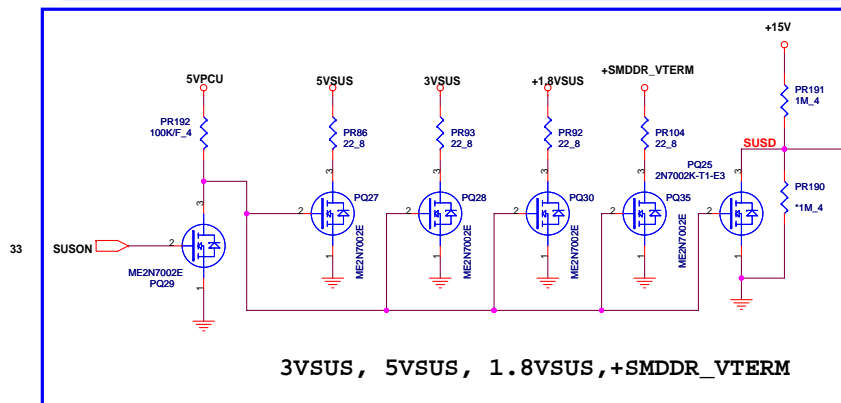


LANVCC

CPU_CORE



3VSUS, 5VSUS, 1.8VSUS, +SMDDR_VTERM



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PROJECT : Congo

Size	Document Number	Rev
	Discharge	1A
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PAGE#	DESCRIPTION	NOTE	PAGE#	DESCRIPTION	NOTE
1	BLOCK DIAGRAM		36	1.2V/1.1V (RT8204)	
2	CLK_GEN_SLG8SP628		37	VCore(MAX8799)	
3	K8G BGA HT I/F 1/4		38	Discharge	
4	K8G BGA DDR2 MEMORY I/F 2/4		39	SYSTEM INFORMATION	
5	K8G BGA CTRL & DEBUG 3/4		40	Power On Sequence	
6	K8G BGA PWR & GND 4/4		41	FL3B Pos Sequence Timing	
7	RS780-HT/PCIE/SPMEM I/F 1/3		42	EC Tracking Record A	
8	RS780-SYSTEM/STRAPS I/F 2/3				
9	RS780-POWER/GND 3/3				
10	SB710-PCIE/PCI/CPU/LPC 1/4				
11	SB710-ACPI/GPIO/USB/AZ 2/4				
12	SB710-SATA/IDE/HWM/SPI3/4				
13	SB710-PWR/DECOUPLING 4/4				
14	SB710-STRAPS & PWRGD				
15	DDR2 SODIMMS & TERMINATOR				
16	LCD/CAMERA				
17	CRT CONN				
18	AUDIO (ALC269VB, SPK)				
19	LAN(RTL8103EL/8111DL)				
20	SATA				
21	USB x 3				
22	Card Reader-RTL5159				
23	WLAN				
24	WWAN				
25	BT/G-SENSOR/TPM				
26	KB/TP				
27	SW/LED/RFID_EEPROM				
28	FAN/Thermal				
29	KBC IT8502E				
30	Screw Hole/EMI				
31	Charger (ISL88731A)				
32	3V/5V (ISL6237)				
33	DDR 1.8V(TPS51116)				
34	VCC1.5 / VCC2.5 (RT9025)				
35	NB_CORE (MAX8792)				

RS780 SM BUS

RS780 I2C (S0)	I2C and AUX Function Define
DAC_SCL DAC_SDA	CRT (+5V)
I2C_CLK I2C_DATA	LVDS (+3V)
DDC_CLK0/AUX0N DDC_DATA1/AUX0P	HDMI (+5V)
DDC_CLK1/AUX1N DDC_DATA1/AUX1P	not used

SB710 SM BUS

SB710 SMBUS	SMBUS Function Define
SMBCLK0 SMBDAT0 (+3V)	DDR / DDR THER / CLOCK GEN
SMBCLK1 SMBDAT1 (+3V_S5)	LAN IC/WI-FI
SMBCLK2 SMBDAT2 (+3V_S5)	not used

KBC(EC) SM BUS

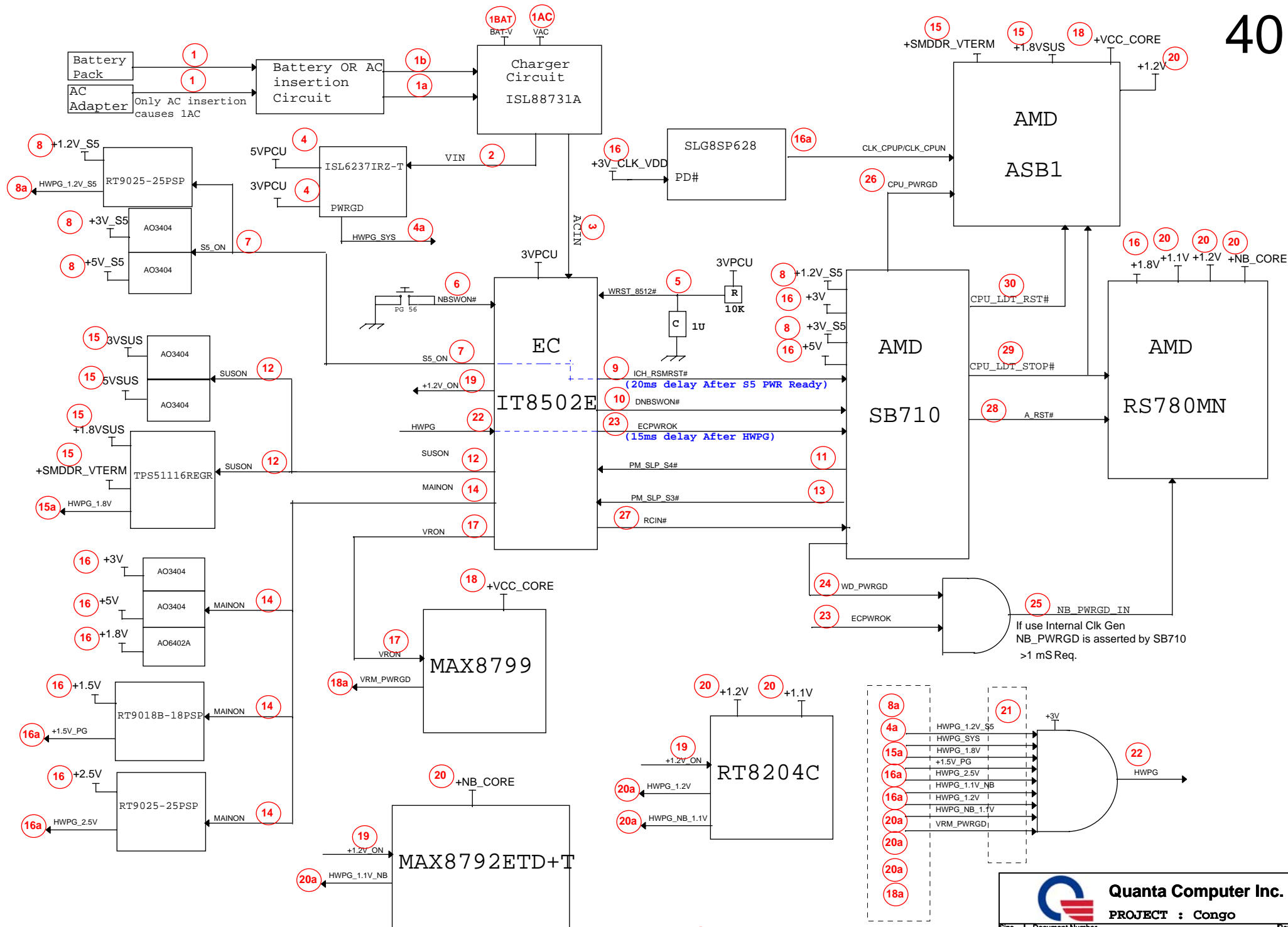
KBC SMBUS (+3VPCU)	SMBUS Function Define
MBCLK MBDAT	BATTERY (+3VPCU)
2ND_MBCLK 2ND_MBDATA	CPU THER SENSOR(+3V) EC EEPROM (+3VPCU)
3ND_MBCLK 3ND_MBDATA	G-SENSOR(+3VS5)

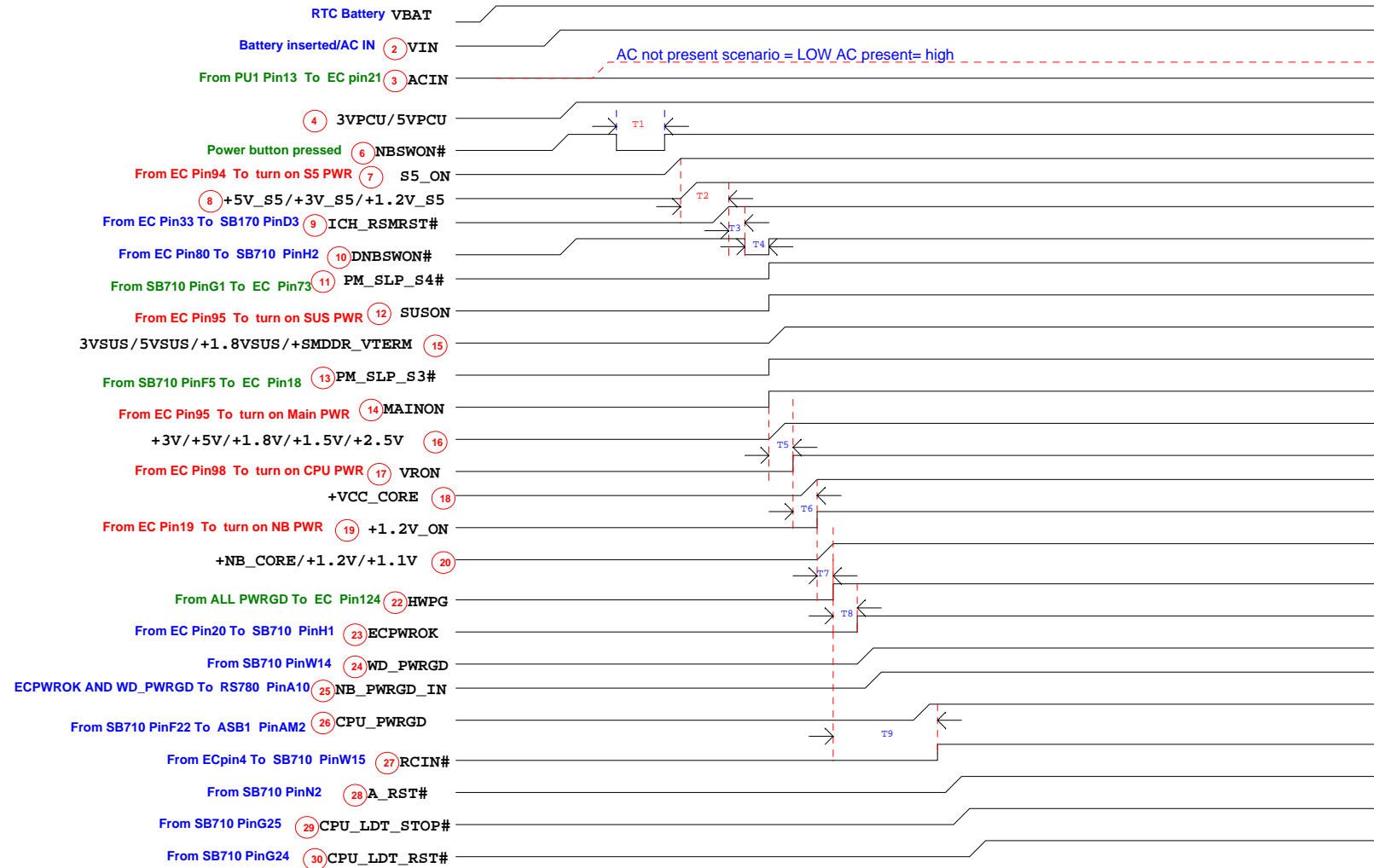


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PROJECT : Congo

Size	Document Number	Rev
	SYSTEM INFORMATION	1A
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T1	>16ms
T2	20ms
T3	5ms
T4	1ms
T5	15ms
T6	5ms
T7	5ms
T8	15ms
T9	108ms

FL3B MK-Note Congo Schematic EC Tracking Record A (for SDV --> SIV)08 /27/ 2009

EC #	Page	CMVC #	Description	Date	Part Affected
A00	31		Change PJ2 pin assignment		
A01	29,11		Change BT_ON# to Test point on EC and BT_ON controlled by SB710 pinW17 (GPIO0)		
A02	26		Change CN8 pin number (13pin-->10pin)		
A03	24		C236 change footprint size		
A04	35		Modify PQ56,PQ57, PL13 footprint		
A05	36		Modify PQ60 footprint		
A06	37		Modify PR165,PR168,PC107,PR17,PR178,PR180 footprint		
A07	27		Delete SW1		
A08	37		Delete PQ53		
A09	32		Delete PJP18,PJP15		
A10	33		Delete PJP16,PJP17		
A11	34		Delete PJP8,PJP6,PJP7		
A12	35		Delete PJP3		
A13	36		Delete PJP5,PJP12		
A14	37		Delete PJP10		
A15	28		Delete Q27 & Mount R344		
A16	05		R73 unmount & Add R416		
A17	05		Exchange Q8 pin1 and pin3 net connection , Unmount R24		
A18	11		Unmount R142,R131,R145,R111 & Mount R143,R132,R139,R110		
A19	22		Change CN10 symbol and footprint		
A20	18		Add CN24 &DIGITAL_MIC Circuit		
A21	21		Unmount R92,R91,R96 & Mount R90,R93		
A22	29		Add MB_ID circuit ,Resume_RST move to default high.(Pin.33-->99) ,Delete D5		
A23	23		C295 change footprint size		
A24	29,21		Add USBCHR_ON# on EC pin97 & U31 pin4		
A25	11		Change USB5--NC,Exchange USB2 & USB4 ,USB5--USB8		
A26	33		Power combustion test need change PQ8 package		
A27	38		Change PR84 from 1M to 100K for fix 3V_S5 knee voltage		
A28	29		Add Wake# signal on EC pin57		
A29	17		Add Pi Filter near CN1 by EMI		
A30	4		Delete Q17,Q18,Q19		
A31	29		Change EC_ID0 signal from EC pin100 to EC pin35		
A32	11		Change R273 to Bead and mount C352		
A33	18		Add R423,R424,R425		
A34	18		Add L-C filter circuit near CN11		
A35	30		HOLE17 connect AGND		
A36	29		Change EC_ID0 signal from EC pin35 to EC pin106 Change EC_ID1 signal from EC pin106 to EC pin35		
A37	27		Reserve for trying LED light on PWR BD with ME		
A38	22		NC R371		
A39	29		Unmount R98		
A40	37		A short pad for EMI		
A41	29		EC Pin76 HDD_DETECT# connect to CN13 Pin12,Change R144 from 10K to 100K.		
A42	20		CN13 Pin12 connect to EC Pin76 HDD_DETECT# ,CN13 Pin18 through a 0 Ohm to GND.		
A43	10		Add D26 for CR2025 (non-chargeable RTC battery)		
A44	3-6		Modify CPU footprint for BGA ball of corner solder mask (open pad size to 14mail) at SIT-R		
A45	7-9		Modify NB footprint for BGA ball of corner solder mask (open pad size to 14mail) at SIT-R		
A46	30		Modify FP of HOLE6 to "H-C259D209P2" for ME.		
A47	16		Modify CAMVCC circuit from 3V to 5V for 5V camera module.		
A48	21		Modify values of ext. R,BOM and modify the power rail of MAX14550A & U5 & U31		
A49	29		Connect EC pin 83 to Flash WP# pin by "EC_WP#",modify BOM for ED_ID table.		
A50	25		Reserve 0 ohm for BT_DET#		
A51	27		Reserve 0603 0ohm for RF solution.		
A52	18		Reserve 0603 0ohm for RF solution.		
A53	10		Reserve charge circuit & Add diode for non-chargeable RTC battery		
A54	32		Change short PJP9 and PJP13 to add Bead (UPB201212T-800Y-N) for RF		
A55	30		Modify FP of HOLE15,HOLE14,HOLE13,HOLE12,HOLE11 for ME.		
A56	10		Change short FP of BT1 for customer request		
A57	29,21		Modify RTS5159 circuit for fix 144 Mhz NOISE		
A58	17,26		Add two 1206 fuse for CRT and Touch Pad		
A59	30		Add 2200p cap *13 for EMI		



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PROJECT : Congo

Size	Document Number	1A
Engineer	Change List	
EC	Thursday, October 22, 2009	1A

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